

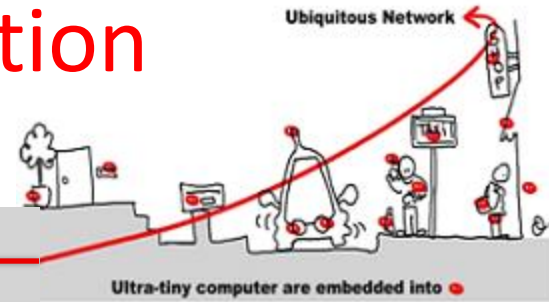
UbiComp Middleware and Verification

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Inria-sam (stars)

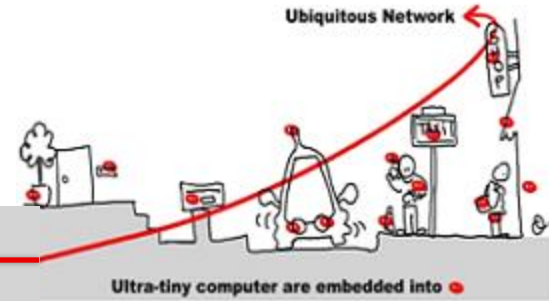
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Ubiquitous Middleware Application Validation



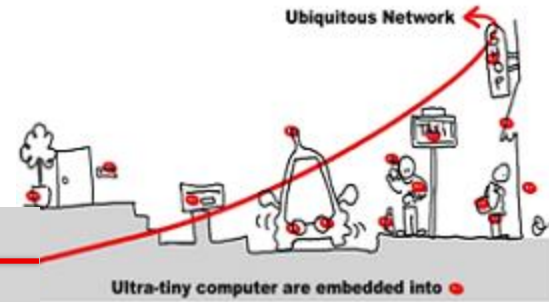
- Ubiquitous and adaptive middleware may be used to design **critical** applications
- Ensure a **safe** usage of these middleware wrt component behavior
- Apply general techniques used to develop **critical software**

Outline



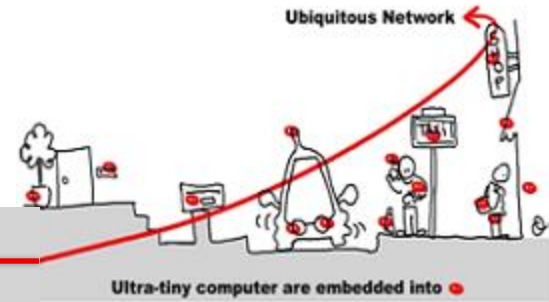
1. Critical system **validation**
2. **Model-checking** solution
 1. Model specification
 2. Model-checking techniques
3. Application to component based adaptive middleware
 1. Middleware critical component as synchronous models to allow validation
 2. The **Scade** solution

Outline



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Critical Software

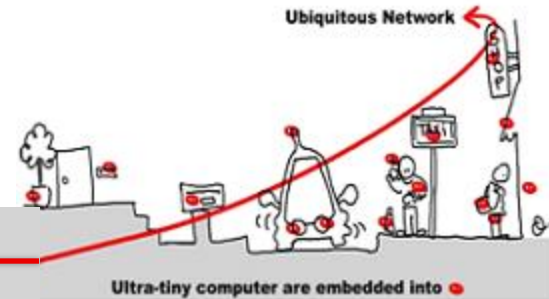


A **critical software** is a software whose failing has **serious consequences**:

- Nuclear technology
- Transportation
 - Automotive
 - Train
 - Aircraft construction

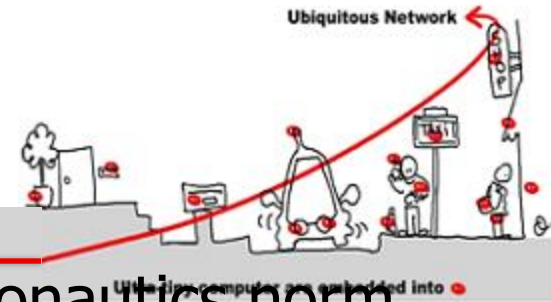
...

Critical Software



- In addition, other consequences are relevant to determine the critical aspect of software:
 - **Financial aspect**
 - Loosing equipment, bug correction
 - Equipment callback (automotive)
 - **Bad advertising**

Software Classification

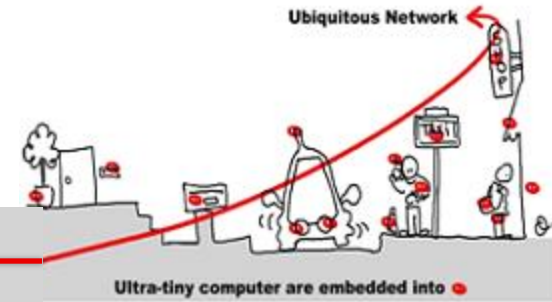


Example of the aeronautics norm DO178B:

- A** **Catastrophic** (human life loss)
- B** **Dangerous** (serious injuries, loss of goods)
- C** **Major** (failure or loss of the system)
- D** **Minor** (without consequence on the system)
- E** **Without effect**

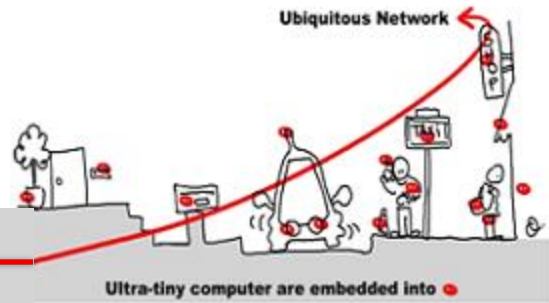
Depending of the level of risk of the system, different kinds of verification are required

Software Classification

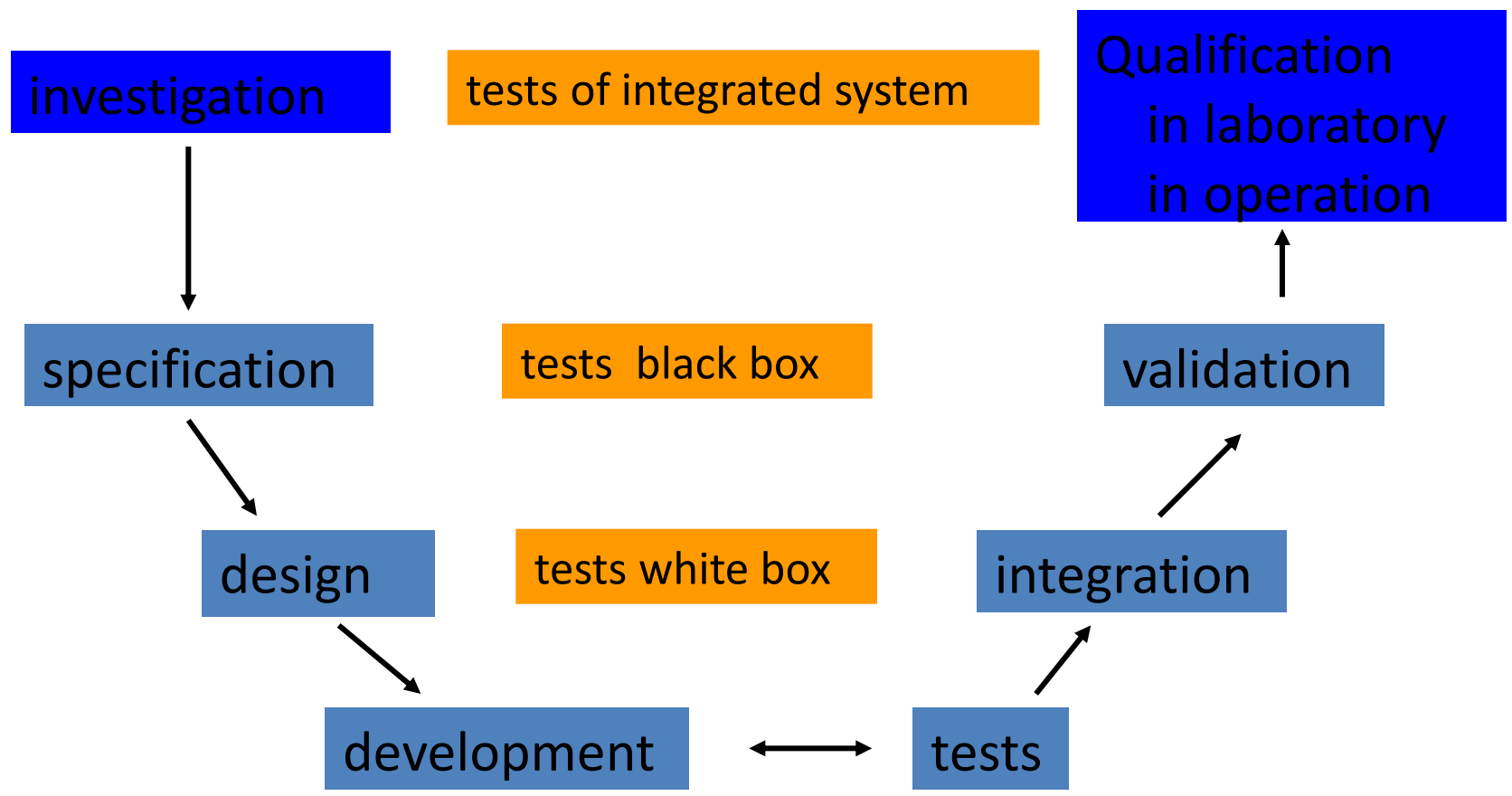


Minor	acceptable situation			
Major				
Dangerous	Unacceptable situation			
catastrophic	$10^{-3} / \text{hour}$	$10^{-6} / \text{hour}$	$10^{-9} / \text{hour}$	$10^{-12} / \text{hour}$
<i>probabilities</i>	probable	rare	very rare	very improbable

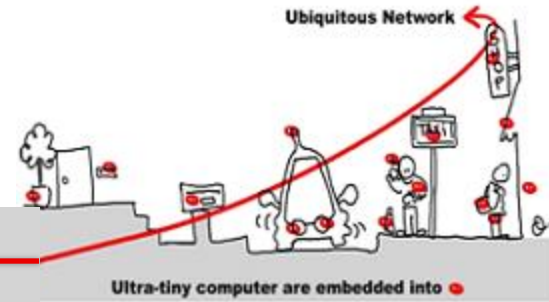
How Develop critical software ?



Classical Development U Cycle

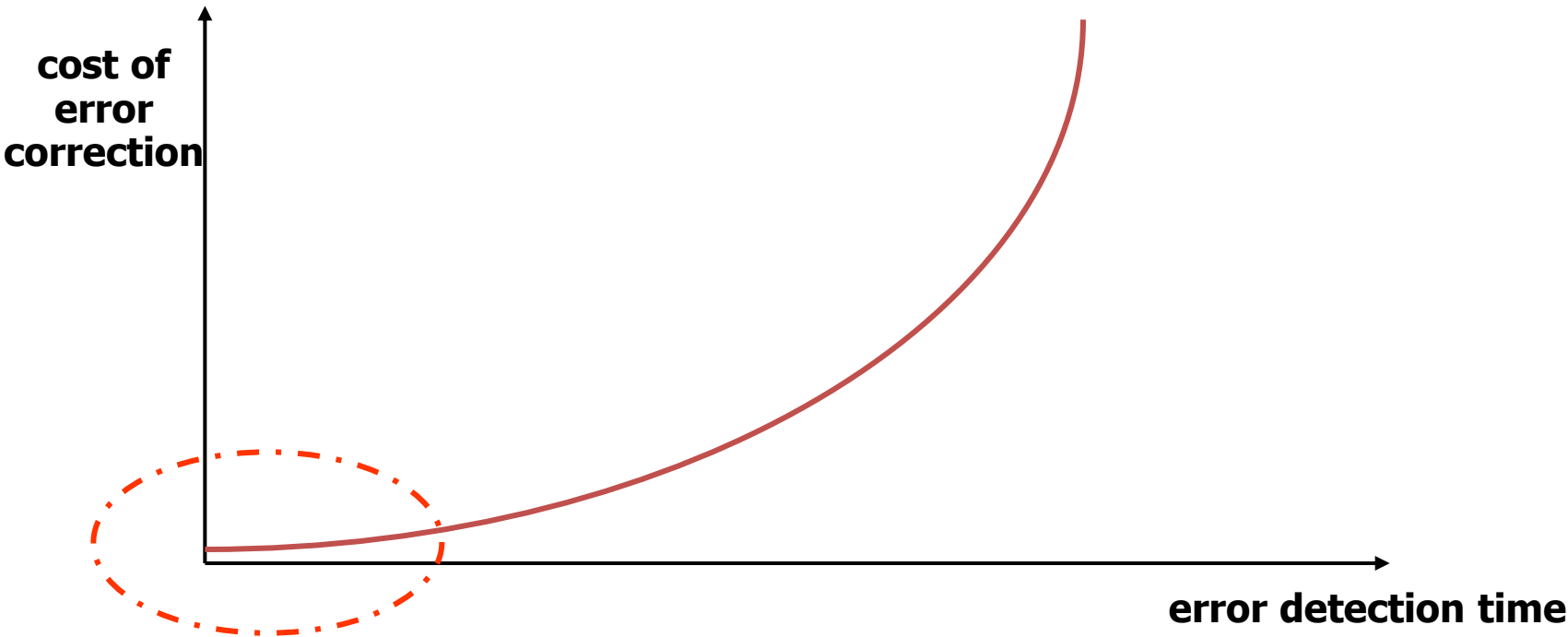
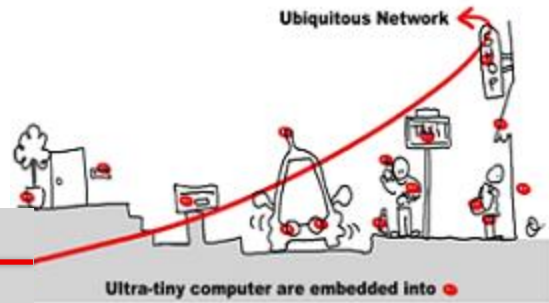


How Develop Critical Software ?



- Cost of critical software development:
 - Specification : 10%
 - Design: 10%
 - Development: 25%
 - Integration tests: 5%
 - Validation: 50%
- Fact:
 - Earlier an error is detected, less expensive its correction is.

Cost of Error Correction

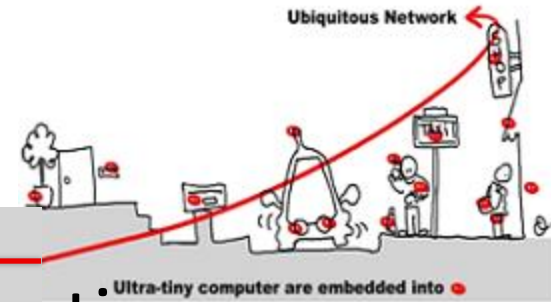


Put the effort on the upstream phase



development based on models

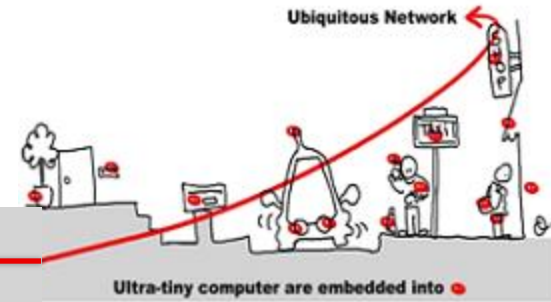
How Develop Critical Software ?



- Goals of critical software specification:
 - Define application needs
 - \Rightarrow **specific domain** engineers
 - Allowing application development
 - **Coherency**
 - **Completeness**
 - Allowing application functional validation
 - Express **properties** to be validated

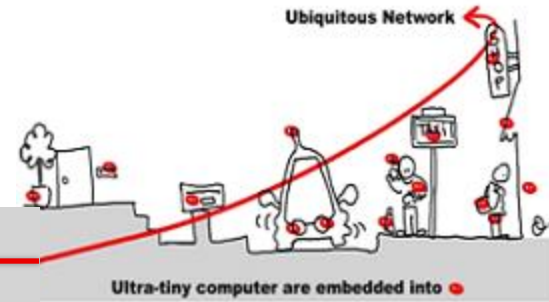
\Rightarrow **Formal model usage**

Critical Software Specification



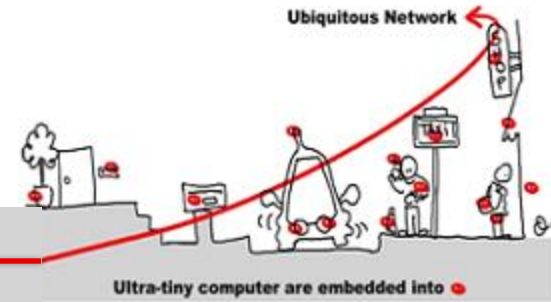
- **First Goal:** must yield a **formal description** of the application needs:
 - Standard to allowing communication between computer science engineers and **non** computer science ones
 - General enough to allow different kinds of application:
 - Synchronous (**and/or**)
 - Asynchronous (**and/or**)
 - Algorithmic

Critical Software Specification

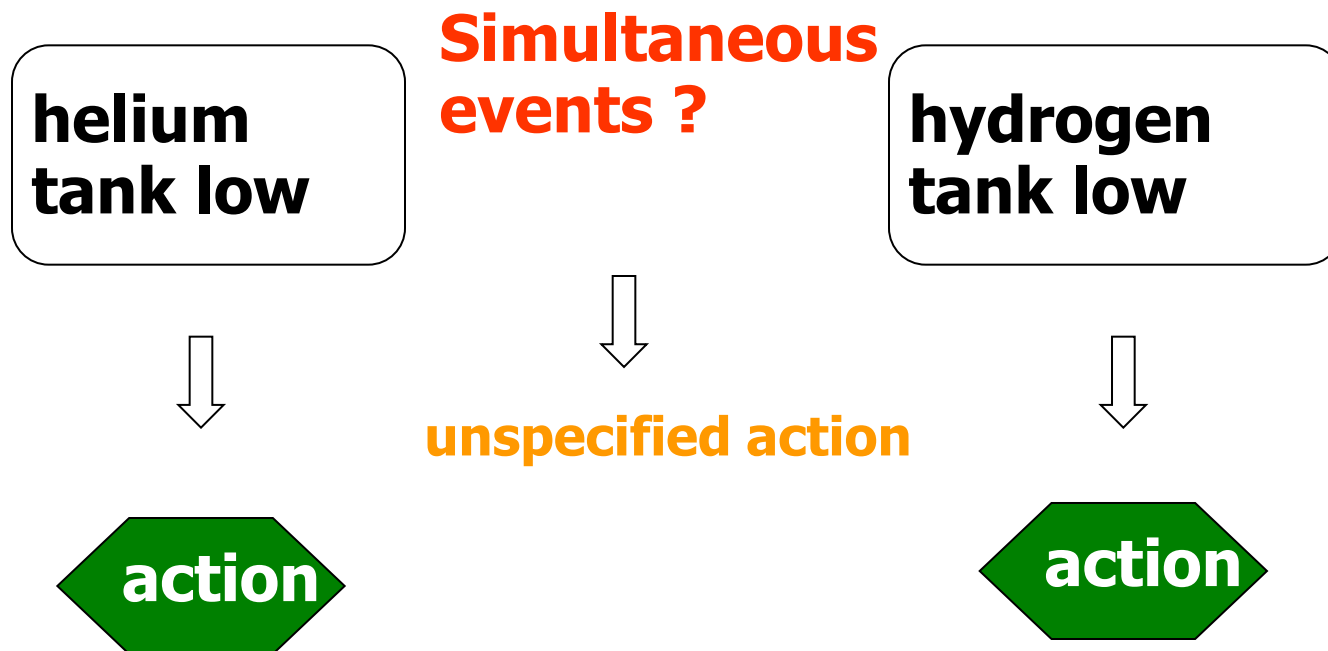


- **Second Goal:** allowing **errors detection** carried out **upstream**:
 - Validation of the specification:
 - Coherency
 - Completeness
 - Proofs
 - Test
 - Quick prototype development
 - Specification simulation

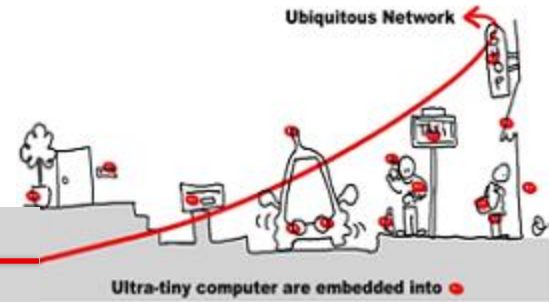
Critical Software Specification



Example of non completeness
From Ariane 5:

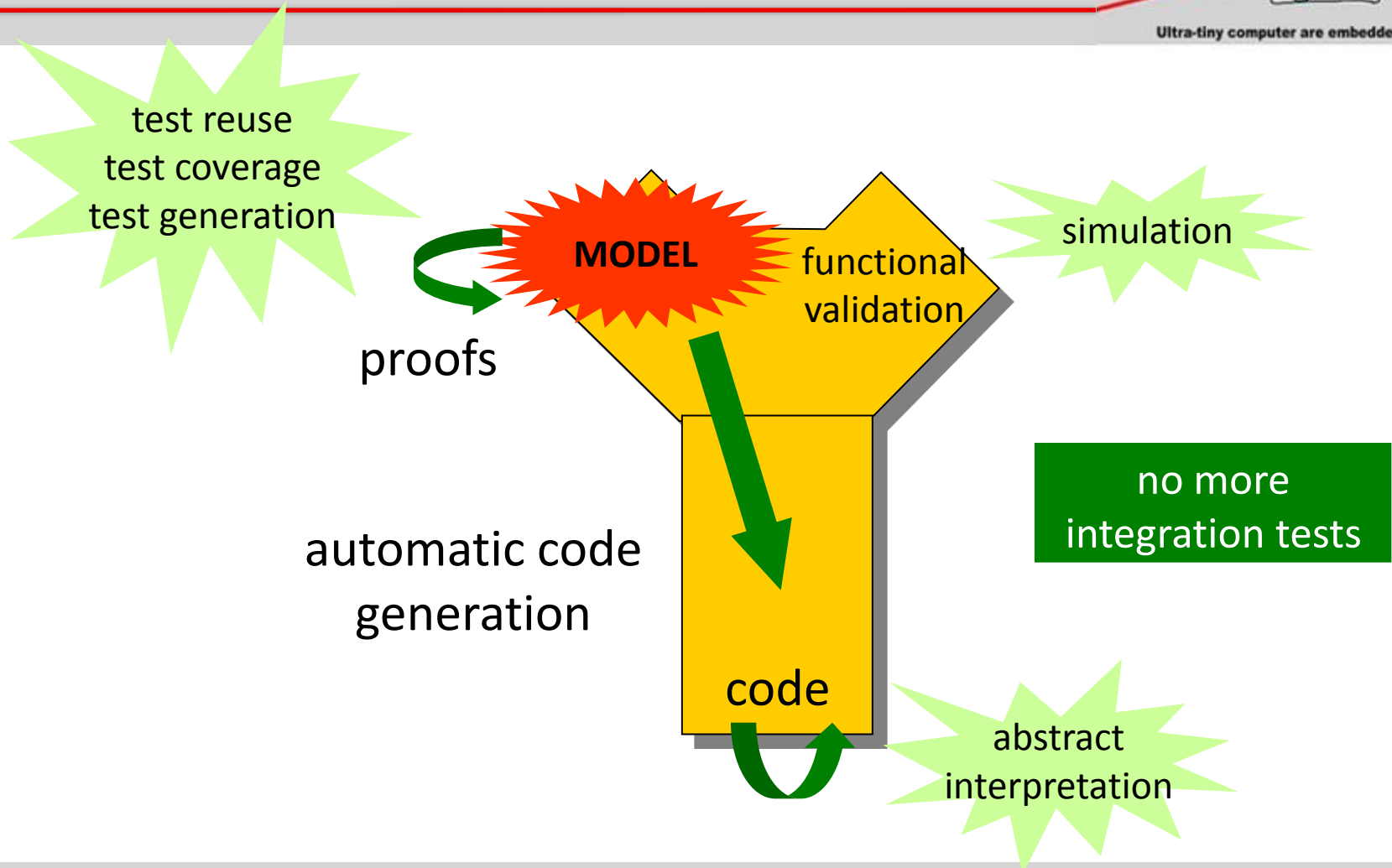
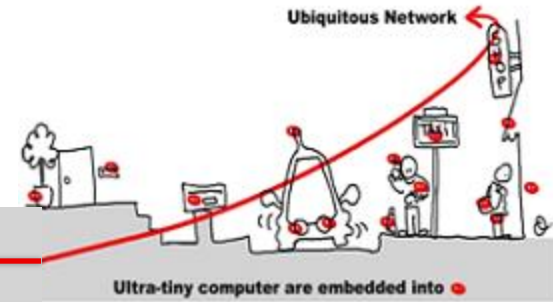


Critical Software Specification

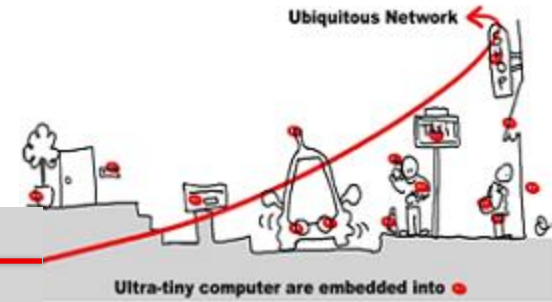


- **Third goal:** make easier the transition from specification to design (**refinement**)
 - Reuse of specification simulation tests
 - Formalization of design
 - **Code generation**
 - Sequential/distributed
 - Toward a target language
 - Embedded/qualified code

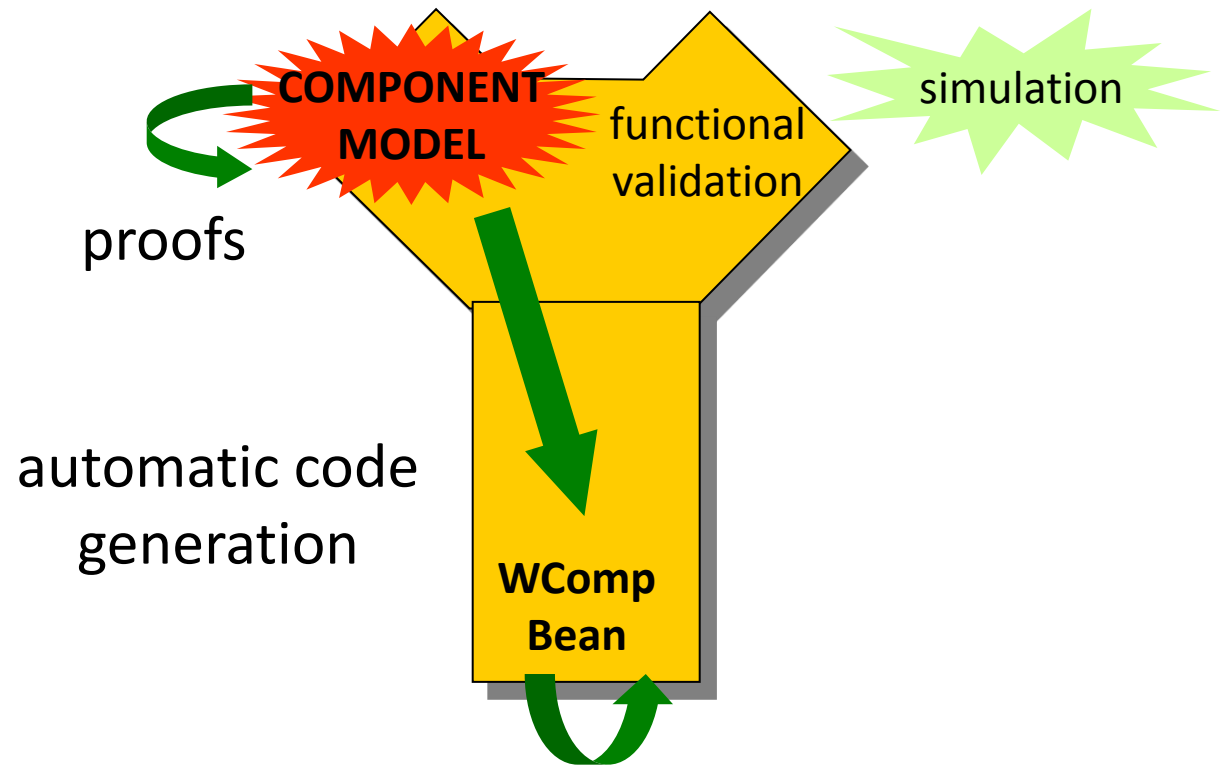
How Develop Critical Software



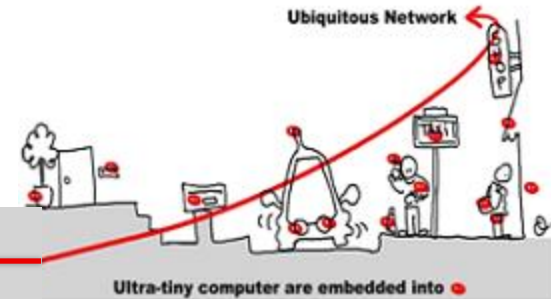
Application to Middleware



In WComp

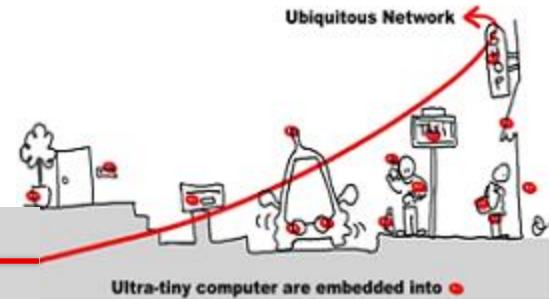


Critical Software Validation



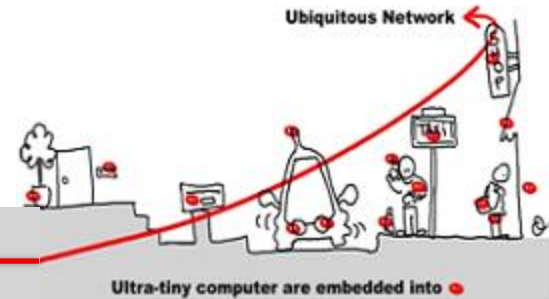
- What is a **correct** software?
 - No execution errors, time constraints respected, compliance of results.
- Solutions:
 - At model level :
 - Simulation
 - Formal proofs
 - At implementation level:
 - Test
 - Abstract interpretation

Validation Methods



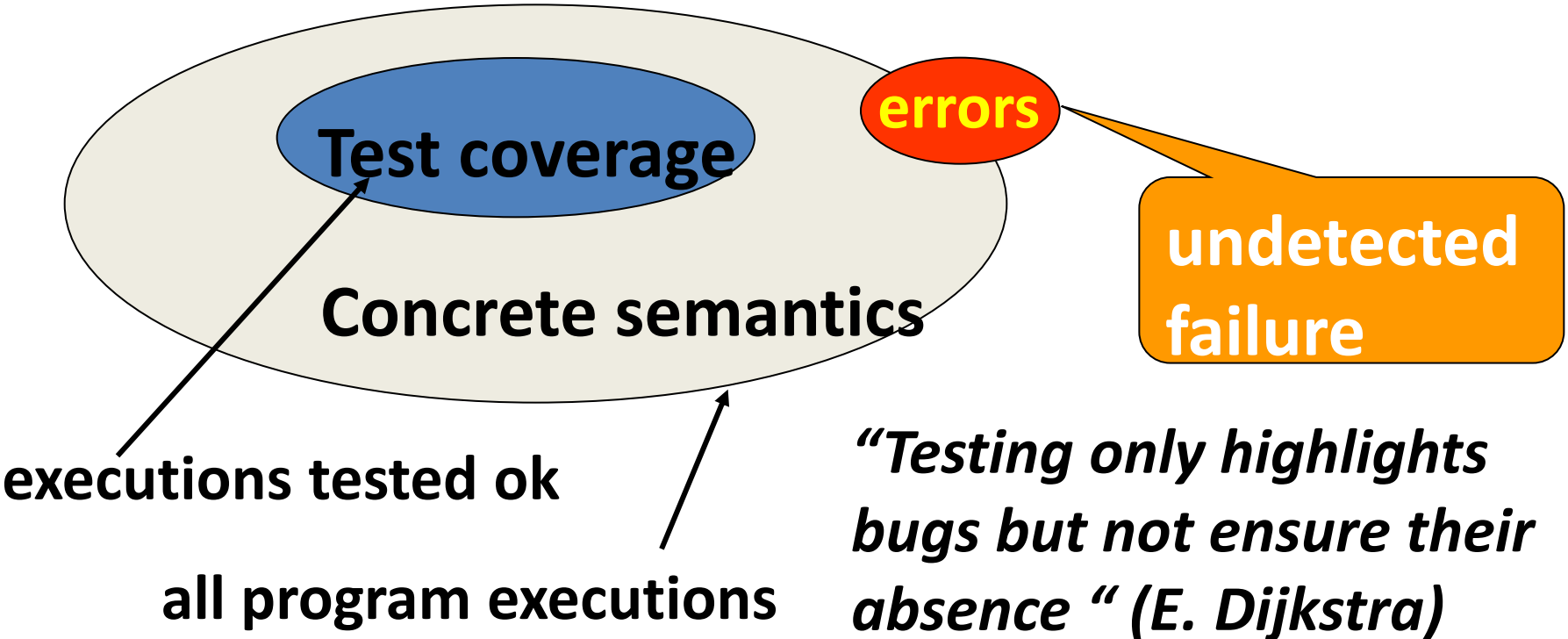
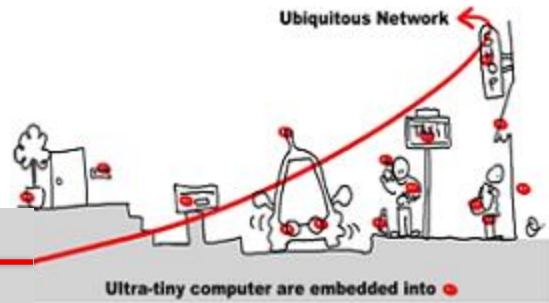
- Testing
 - Run the program on set of inputs and check the results
- Static Analysis
 - Examine the source code to increase confidence that it works as intended
- Formal Verification
 - Argue formally that the application always works as intended

Testing

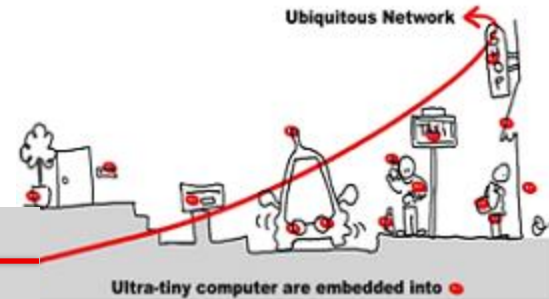


- Dynamic verification process applied at implementation level.
- Feed the system (or one of its components) with a set of input data values:
 - Input data set not too large to avoid huge time testing procedure.
 - Maximal coverage of different cases required.

Program Testing

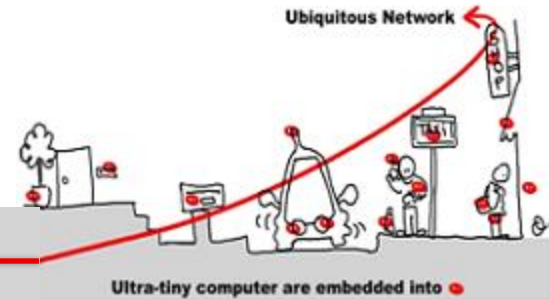


Static Analysis



- The aim of static analysis is to search for errors without running the program.
- *Abstract interpretation* = replace data of the program by an abstraction in order to be able to compute program properties.
- Abstraction must ensure :
 - $\mathbb{A}(P)$ “correct” \Rightarrow P correct
 - But $\mathbb{A}(P)$ “incorrect” \Rightarrow ?

Static Analysis: example



abstraction: integer by intervals

```
1: x := 1;  
2: while (x < 1000) {  
3:   x := x+1;  
4: }
```



$$x1 = [1, 1]$$

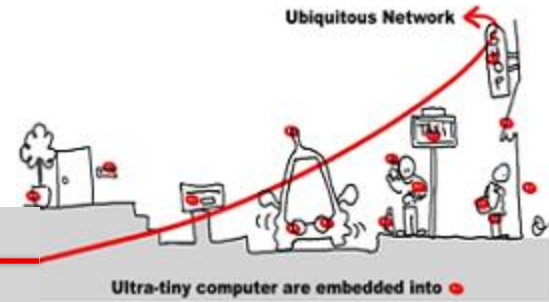
$$x2 = x1 \cup x3 \cap [-\infty, 999]$$

$$x3 = x2 \oplus [1, 1]$$

$$x4 = x1 \cup x3 \cap [1000, \infty]$$

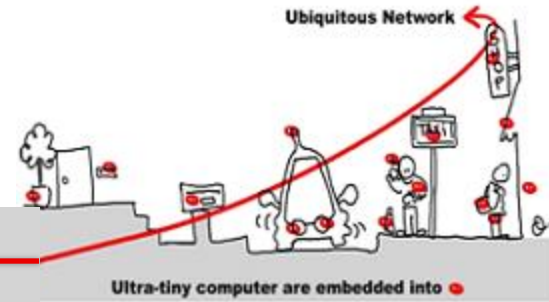
Abstract interpretation theory \Rightarrow values are fix point equation solutions.

Formal Verification



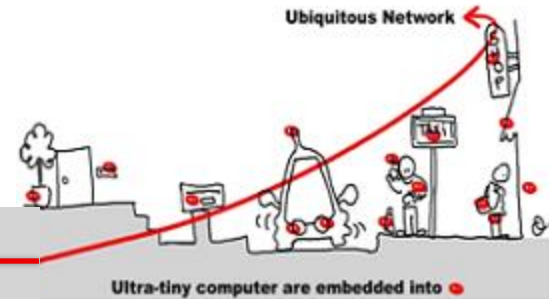
- What about **functional validation** ?
 - Does the program compute the expected outputs?
 - Respect of time constraints (temporal properties)
 - Intuitive partition of temporal properties:
 - **Safety properties**: something bad never happens
 - **Liveness properties**: something good eventually happens

Safety and Liveness Properties



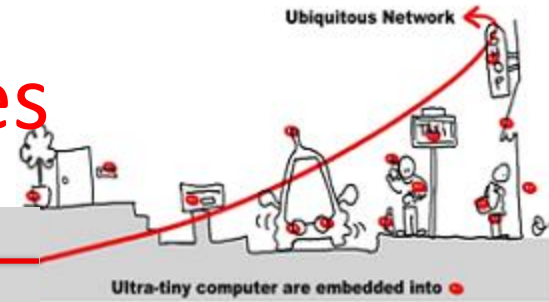
- Example: the beacon counter in a train:
 - Count the difference between beacons and seconds
 - Decide when the train is ontime, late, early
 - **ontime** : difference = 0
 - **late** : difference > 3 and it was ontime before or difference > 1 and it was already late before
 - **early** : difference < -3 and it was ontime before or difference < -1 and it was ontime before

Safety and Liveness Properties



- Some properties:
 1. It is impossible to be late and early;
 2. It is impossible to directly pass from late to early;
 3. It is impossible to remain late only one instant;
 4. If the train stops, it will **eventually** get late
- Properties 1, 2, 3 : **safety**
- Property 4 : **liveness**

Safety and Liveness Properties



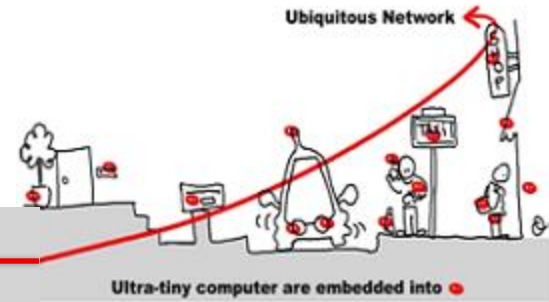
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Properties 1, 2, 3 : **safety**

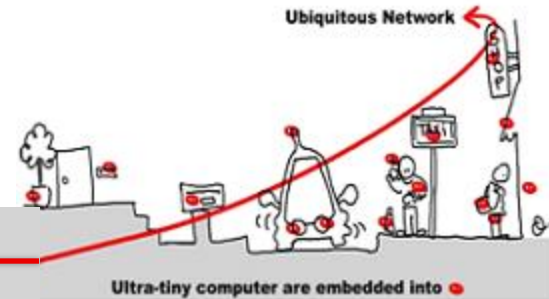
Property 4 : **liveness** (refer to unbound future)

Outline



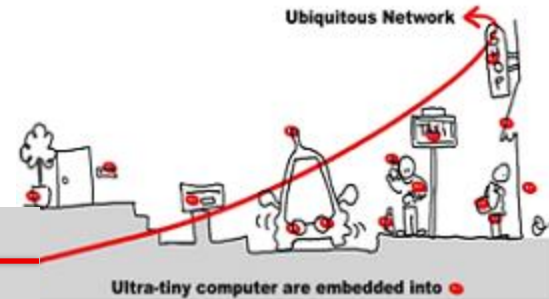
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Safety and Liveness Properties Checking



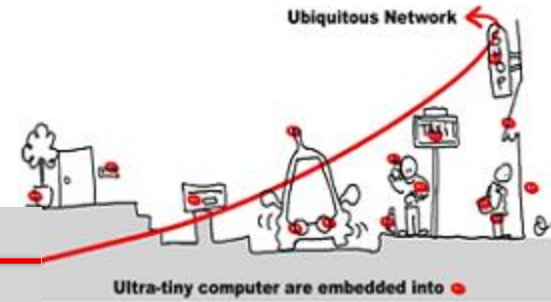
- Use of **model checking** technique
- **Model checking goal**: prove **safety** and **liveness** properties of a system in analyzing a **model** of the system.
- Model checking techniques require:
 - **model** of the system
 - **express** properties
 - **algorithm** to check properties against the model (\Rightarrow **decidability**)

Model Checking Techniques



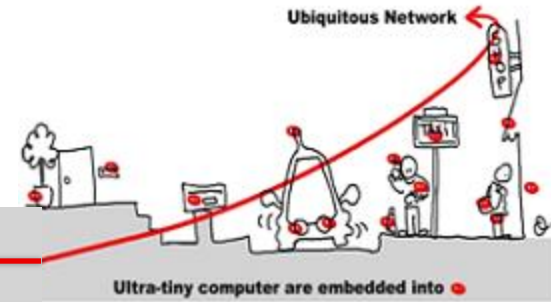
- **Model** = automata which is the set of program behaviors
- **Properties expression** = **temporal logic**:
 - **LTL** : liveness properties
 - **CTL**: safety properties
- **Algorithm** =
 - LTL : algorithm exponential wrt the formula size and linear wrt automata size.
 - CTL: algorithm linear wrt formula size and wrt automata size

Model Checking Model Specification



- **Model** = automata which is the set of program behaviors

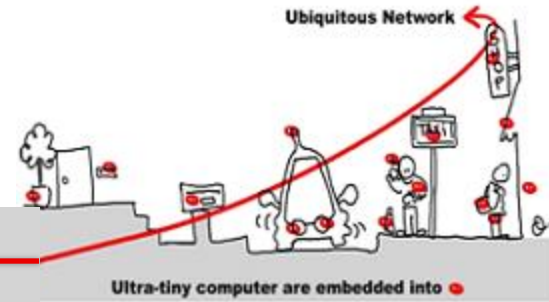
Model Specification



- **Model** = automata which is the set of program behaviors
- An automata is composed of:
 1. A finite set of states (Q)
 2. A finite alphabet of actions (\mathbb{A})
 3. An initial state ($q^{\text{init}} \in Q$)
 4. A transition relation (\mathbb{R} in $Q \times Q$)
 5. A labeling function $\lambda : Q \times Q \rightarrow \mathbb{A}$

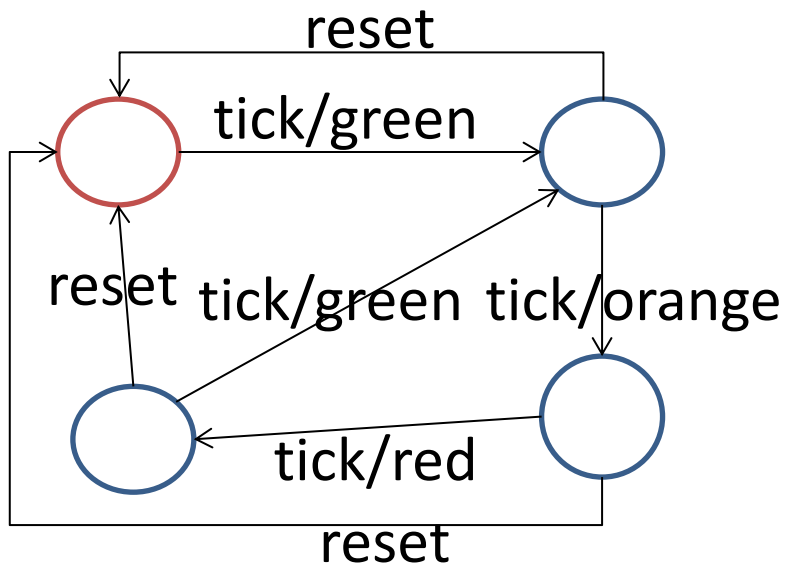
Notation: a transition is denoted $q_1 \xrightarrow{a} q_2$

Model Specification



- **Model** = automata which is the set of program behaviors

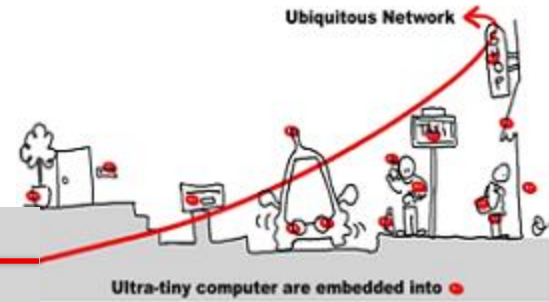
Example: Traffic Light



trigger: tick, reset

action: green, orange, red

Model Checking

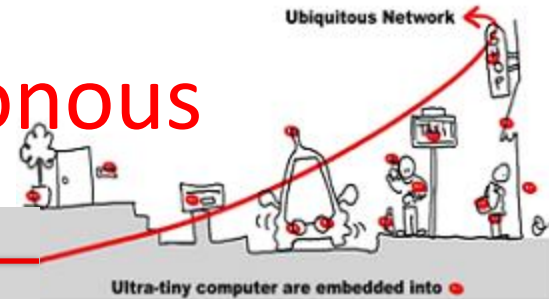


How design automata as system behaviors ?

Use **synchronous languages** to specify critical systems.

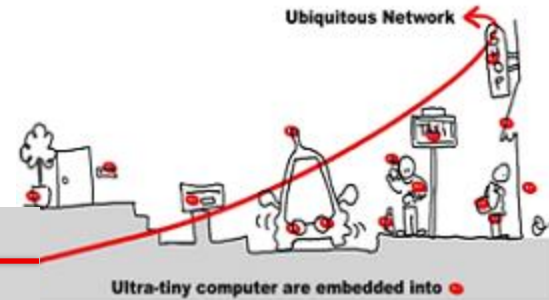
Synchronous programs = automata

Model Specification with Synchronous Languages



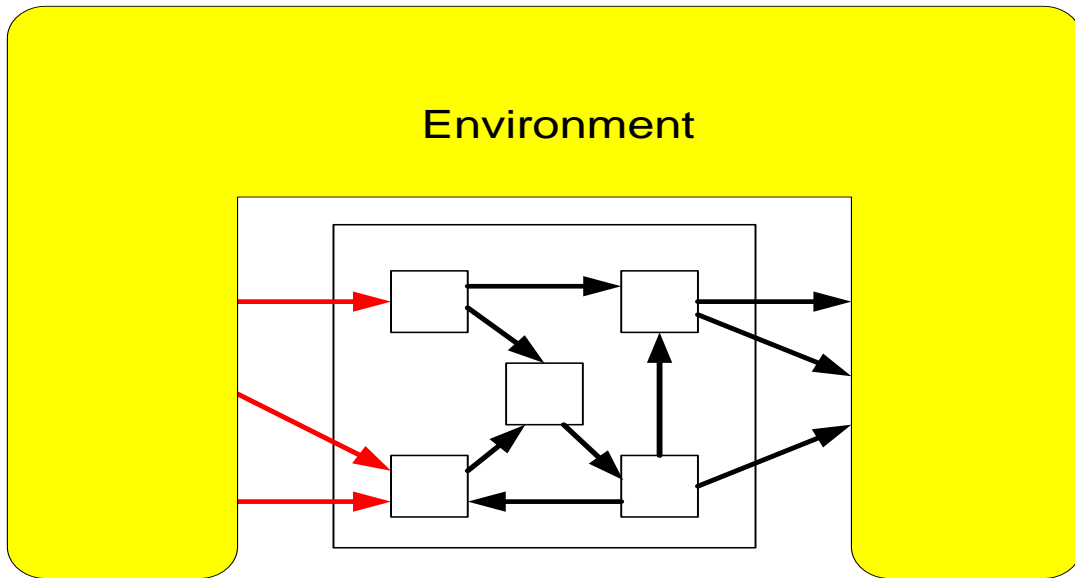
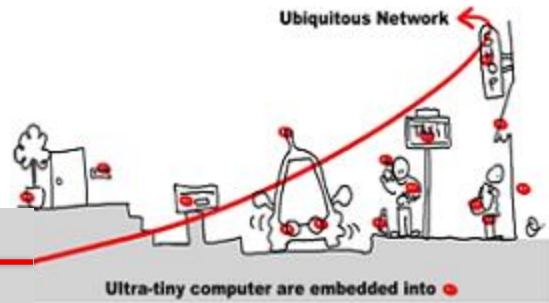
1. Synchronous languages have a **simple formal model** (a finite automaton) making formal reasoning tractable.
2. Synchronous languages support **concurrency** and offer an implicit or explicit means to express parallelism.
3. Synchronous languages are devoted to design **reactive systems**.

Determinism & Reactivity



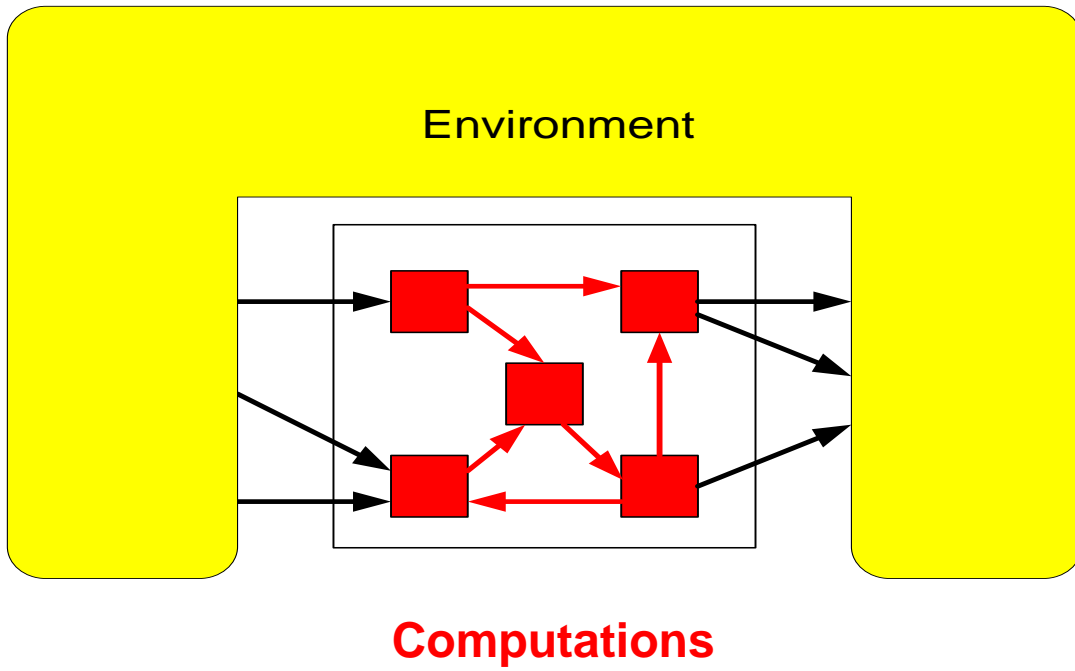
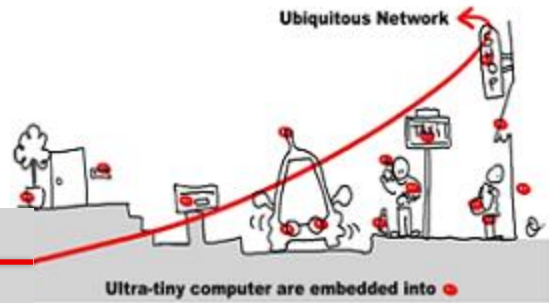
- Synchronous languages are deterministic and reactive
- Determinism:
 - The same input sequence always yields the same output sequence
- Reactivity:
 - The program must react^(*) to any stimulus
 - Implies absence of deadlock
 - (*) Does not necessary generate outputs, the reaction may change internal state only.

Synchronous Reactive Programs (1)

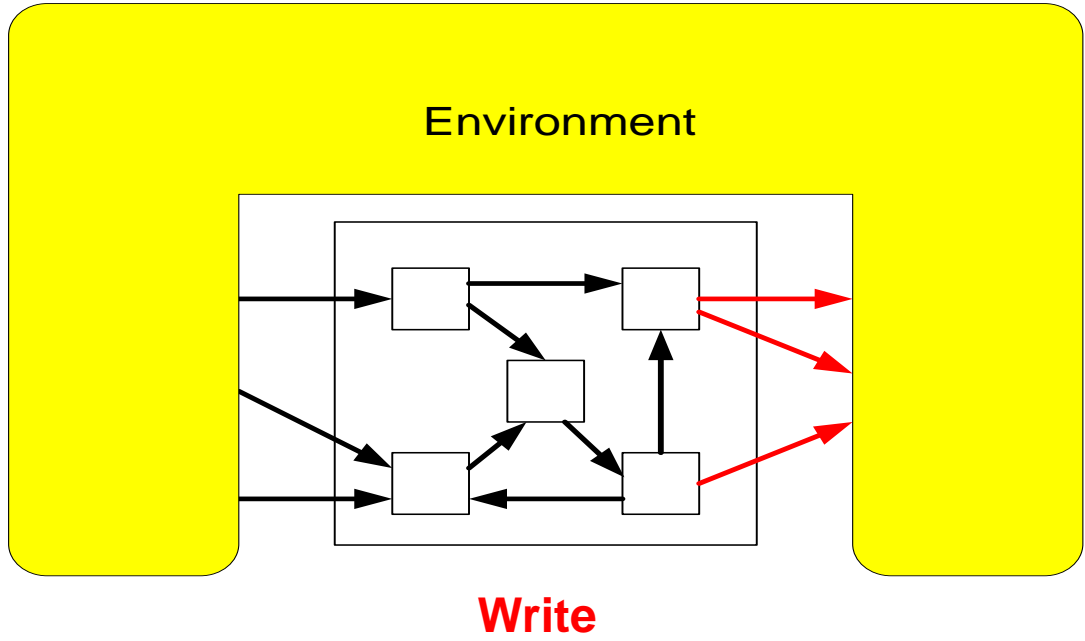
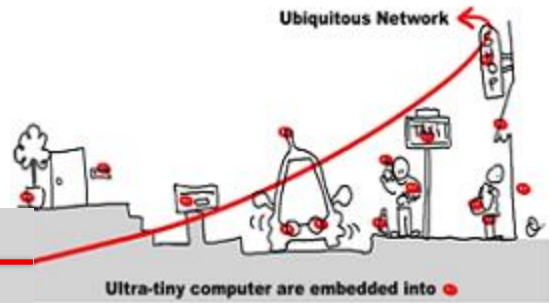


Read

Synchronous Reactive Programs (1)

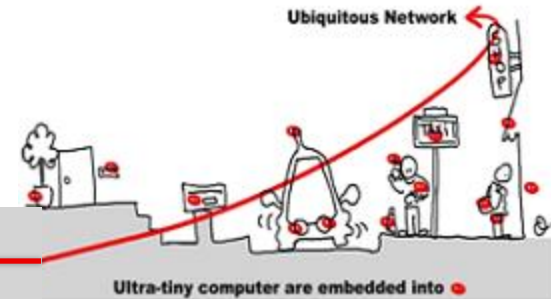


Synchronous Reactive Programs (1)



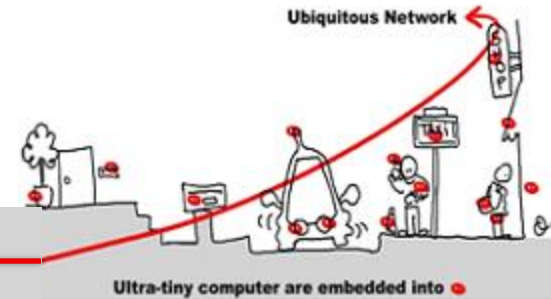
Atomic execution: read, compute, write

Synchronous Hypothesis



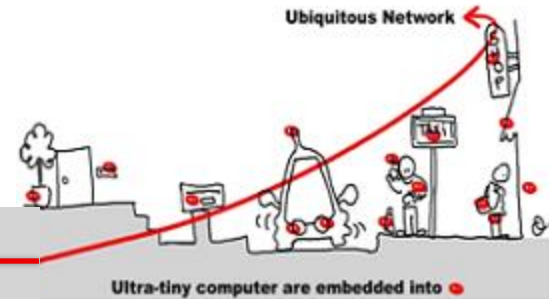
- Synchronous languages work on a **logical time**.
 - The time is
 - Discrete
 - Total ordering of **instants**.
- } Use N as time base
- A reaction executes in one instant.
 - Actions that compose the reaction may be partially ordered.

Synchronous Hypothesis



- **Communications** between actors are also supposed to be **instantaneous**.
- All parts of a synchronous model **receive exactly the same information** (instantaneous broadcast).
- Outcome: Outputs are simultaneous with Inputs (they are said to be **synchronous**)
- Thanks to these strong hypotheses, **program execution is fully deterministic**.

Reactive ?



- Different ways to “react” to the environment:

- **Event** driven system:

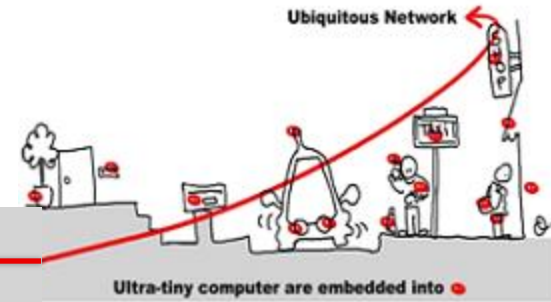
- Receive events
- Answer by sending events

- **Data flow** system:

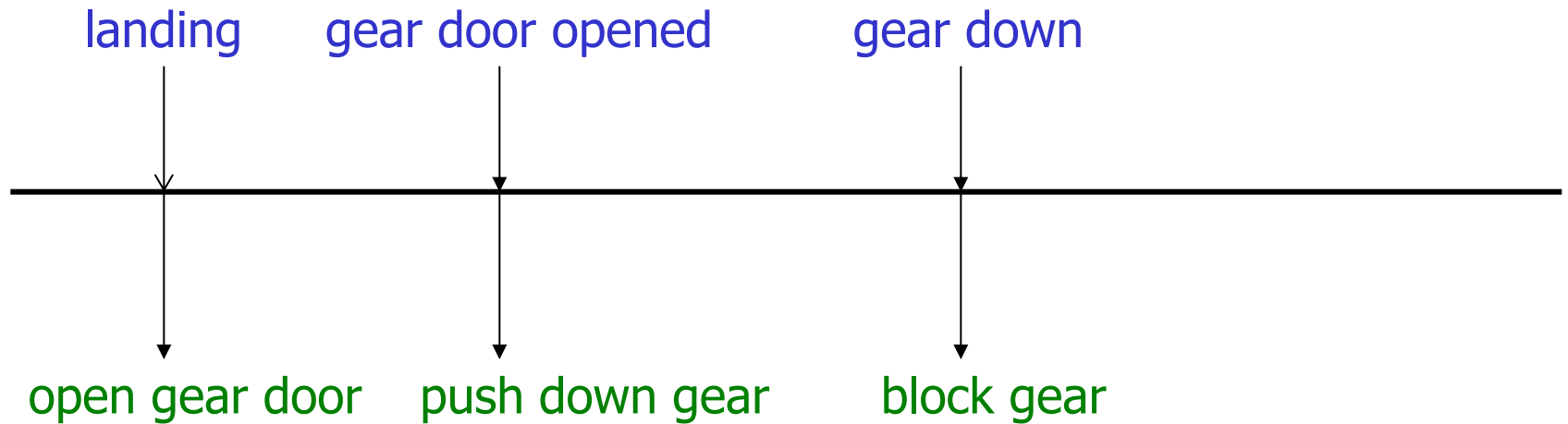
- Receive data continuously
- Answer by treating data continuously also

**Some systems
have components of
both kinds**

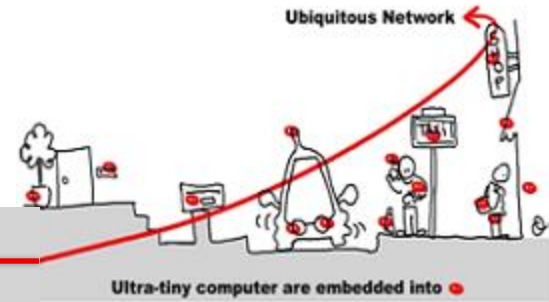
Event Driven Reactive System



Langing gear management



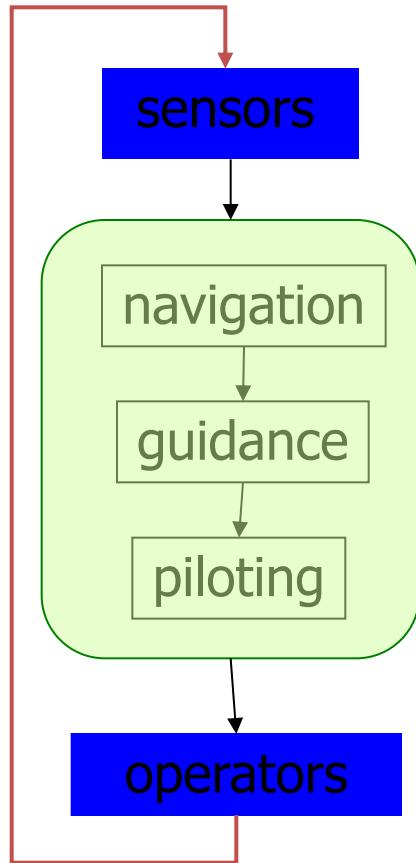
Data Flow Reactive System (Example)



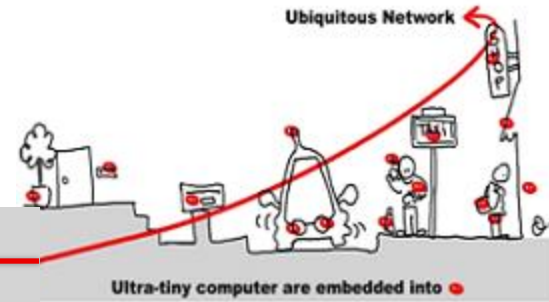
Control/Command vehicle

- get measures
- where am I ?
- where go I ?
- command computation
- command to operators

Periodic processus

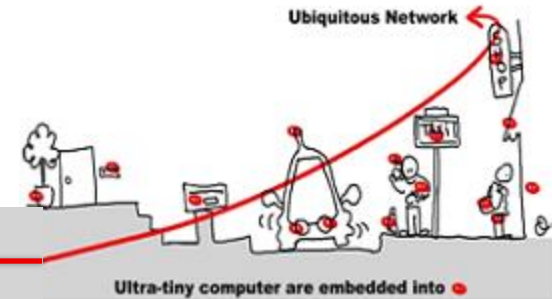


Imperative and Declarative languages



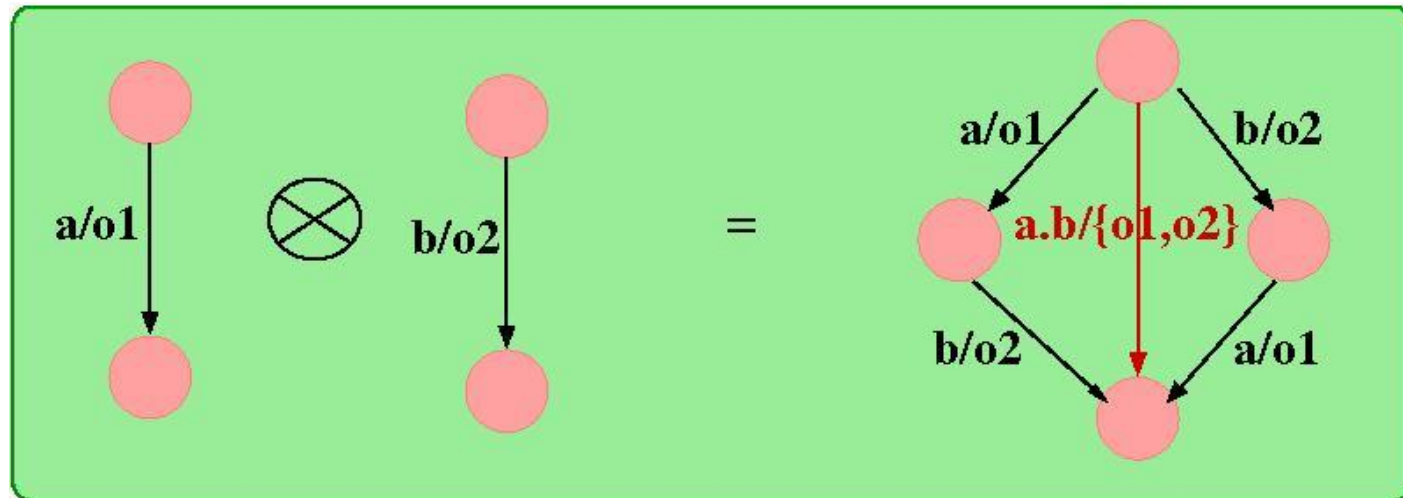
- Different ways to express synchronous programs:
 1. Imperative languages rely on implicitly or explicitly **finite state machines**, well suited to design event driven reactive system
 2. Declarative languages rely on operator networks computing **data flows**, well suited to design data flow reactive system

Event Driven = FSM

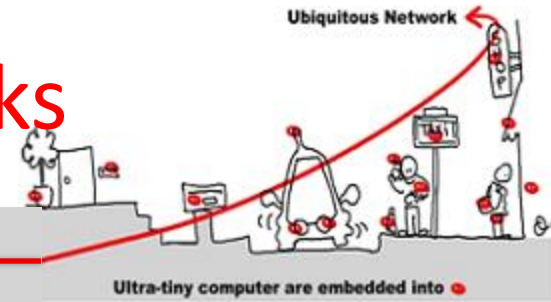


Event driven applications can be designed:

1. As simple finite state machines (= automata)
2. As the **synchronous product** of finite state machines

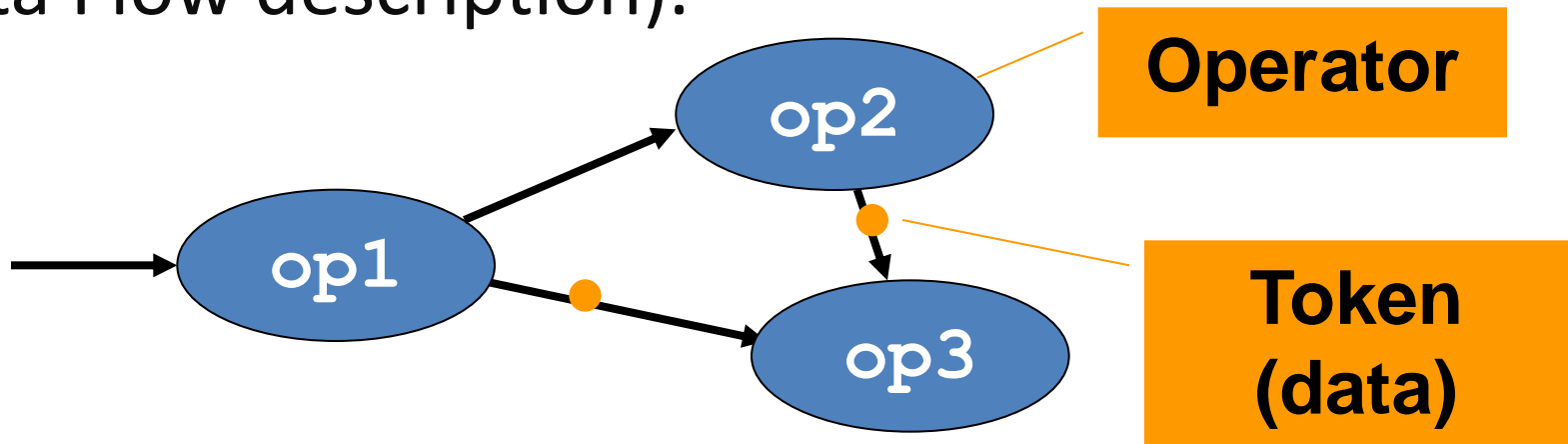


Data flow = Operator Networks

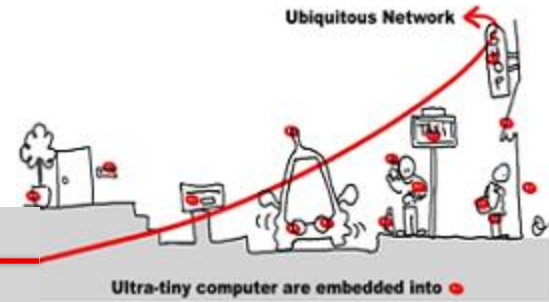


Data flow programs can be interpreted as **networks of operators**.

Data « flow » to operators where they are consumed. Then, the operators generate new data. (Data Flow description).



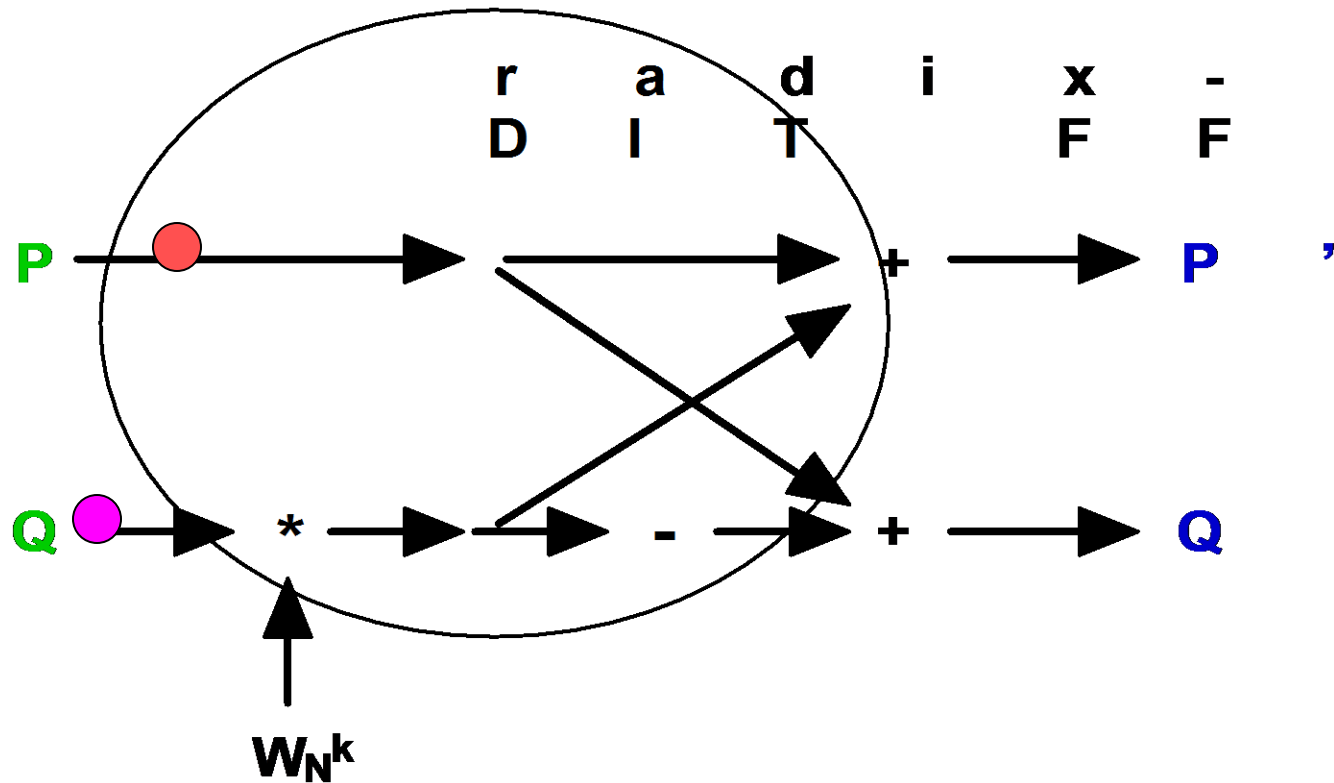
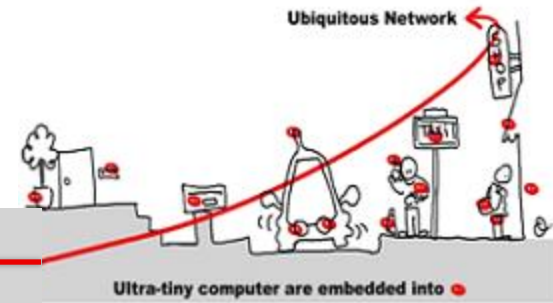
Flows, Clocks



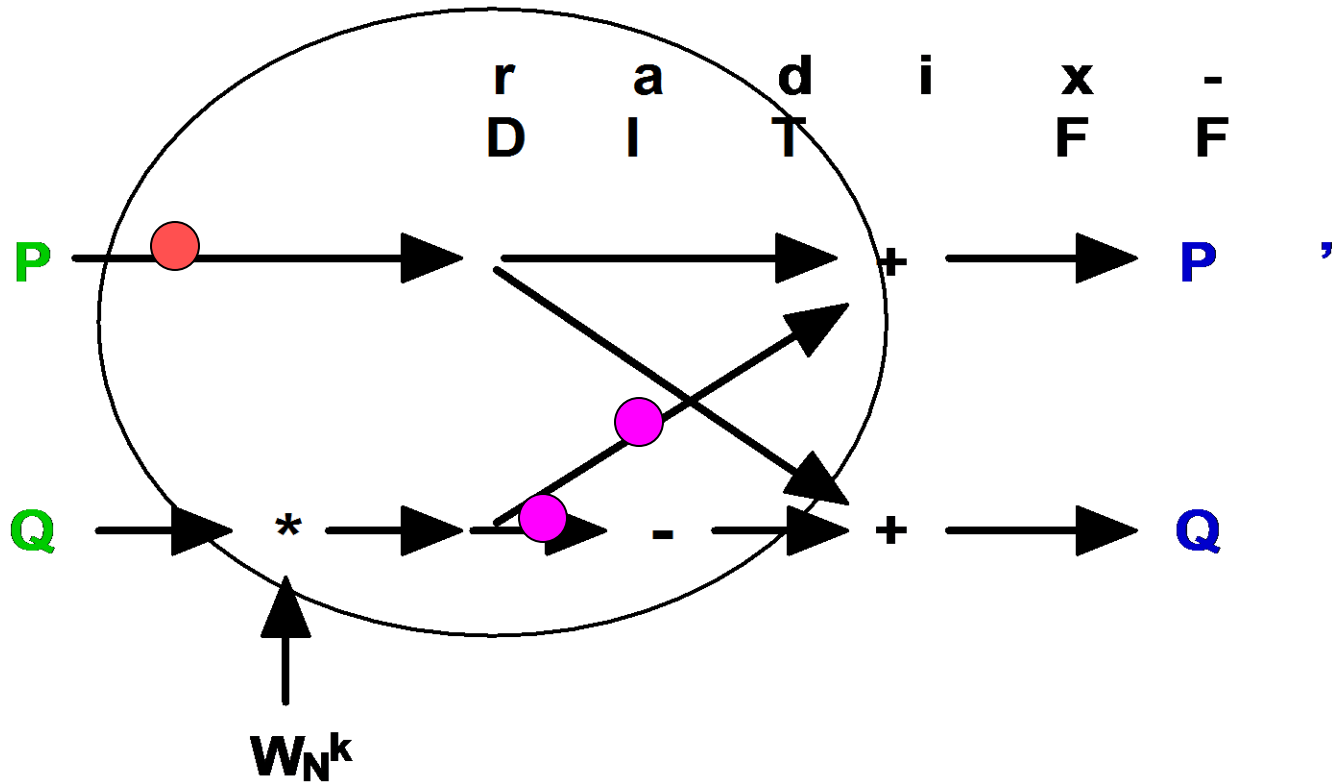
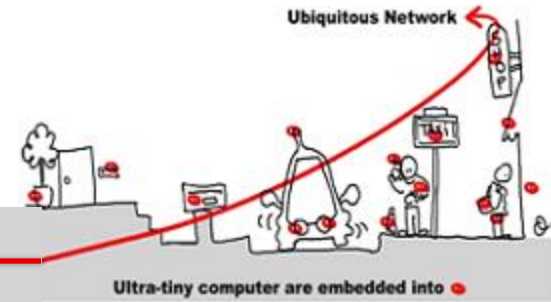
- A **flow** is a pair made of
 - A possibly infinite sequence of **values of a given type**
 - A **clock** representing a sequence of **instants**

$$X:T \quad (x_1, x_2, \dots, x_n, \dots)$$

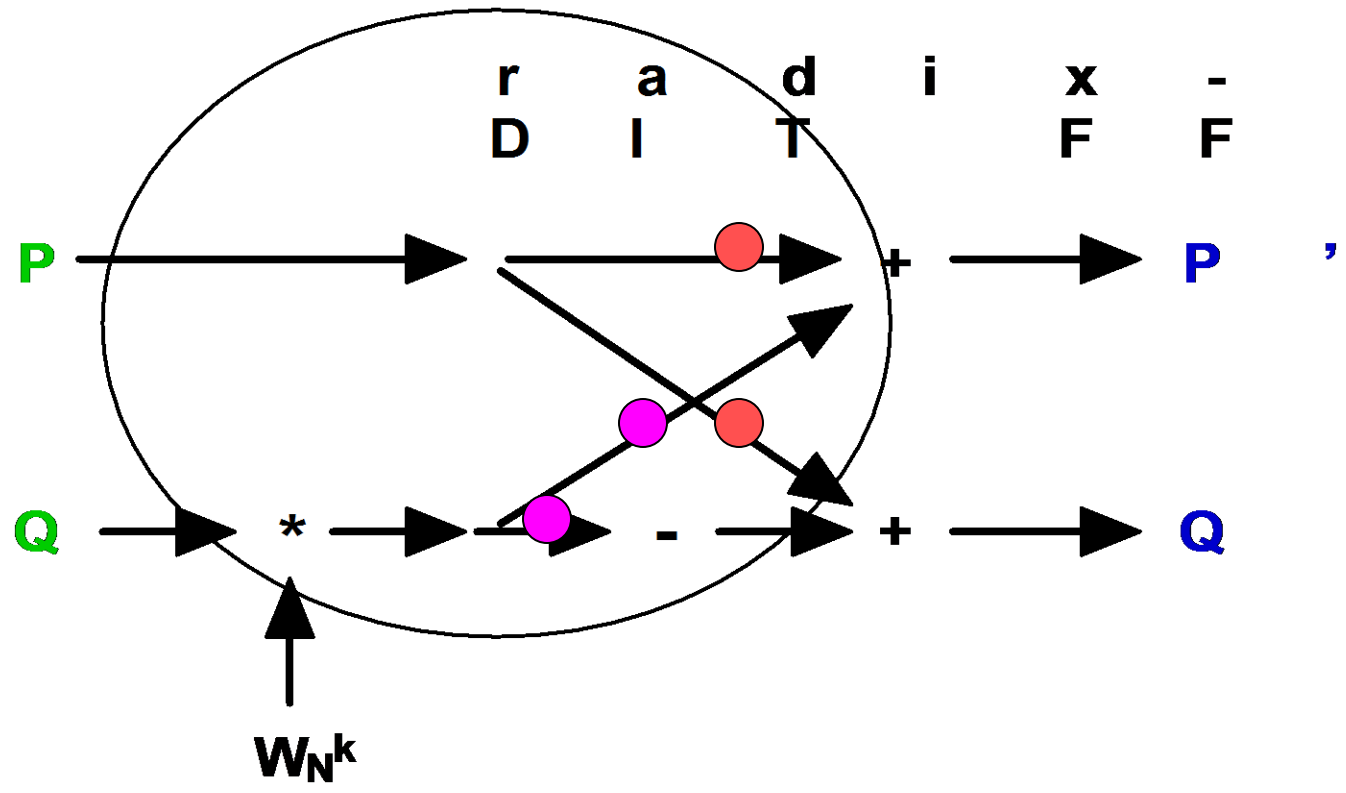
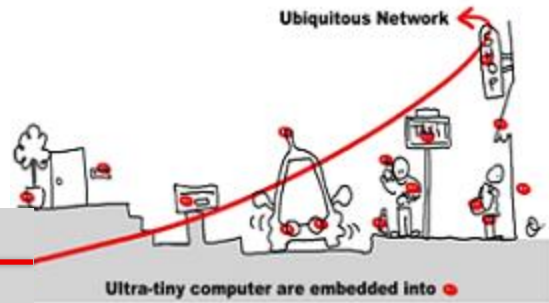
An example of Data Flow



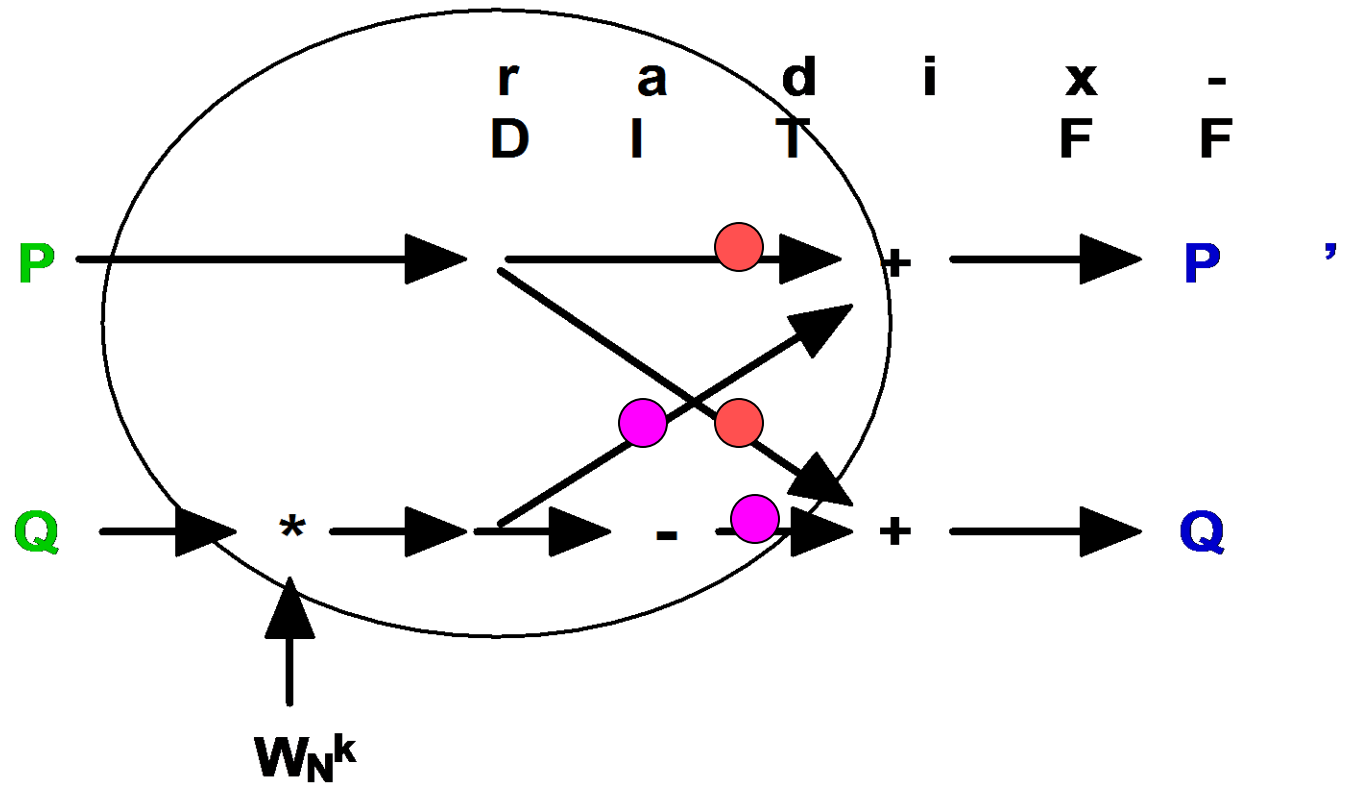
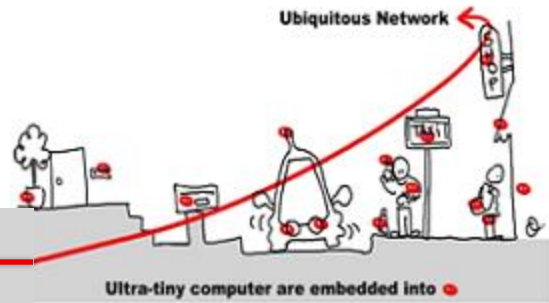
Data Flow



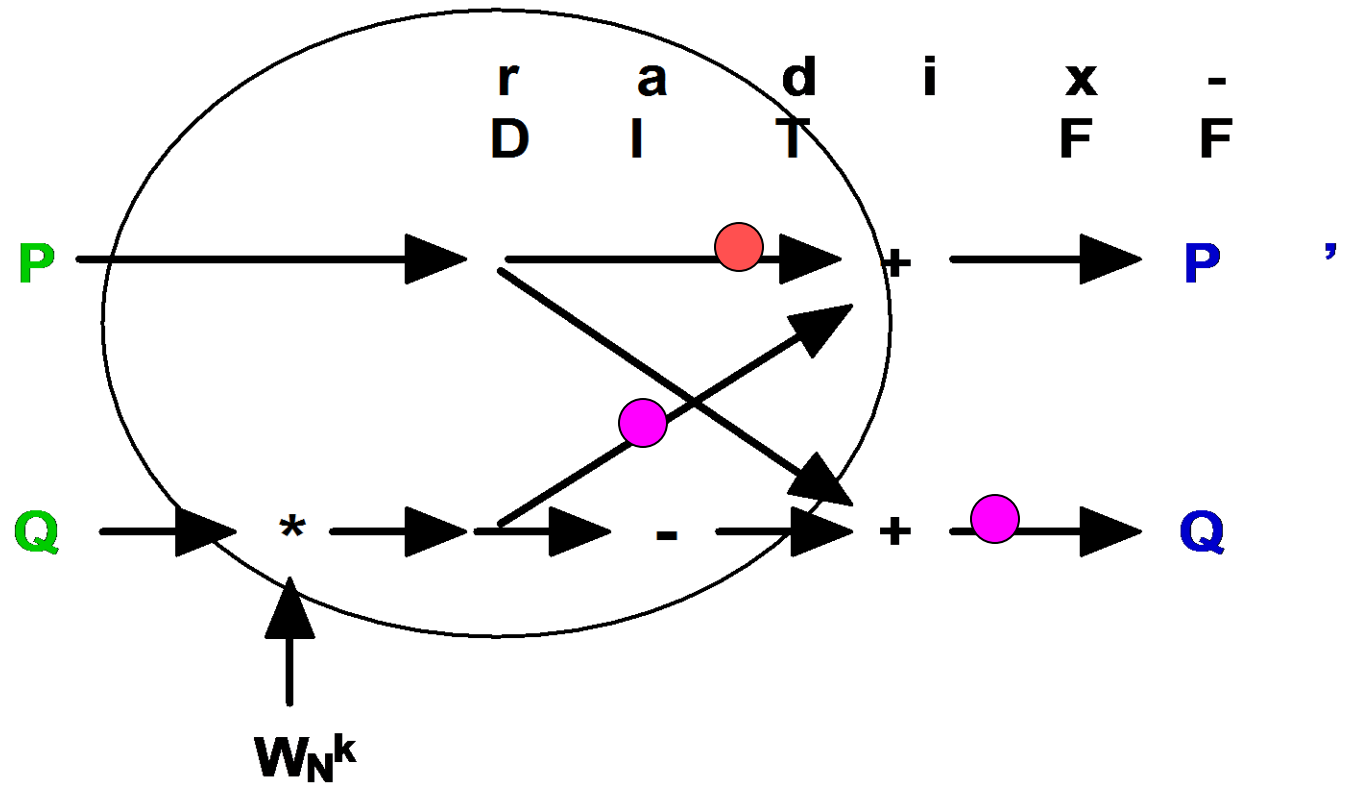
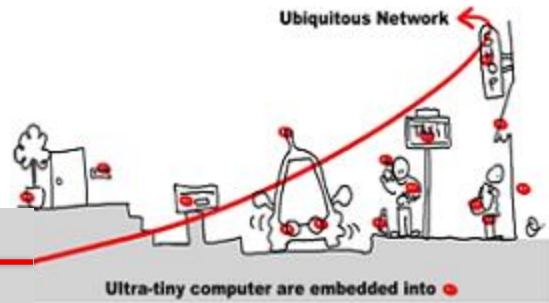
Data Flow



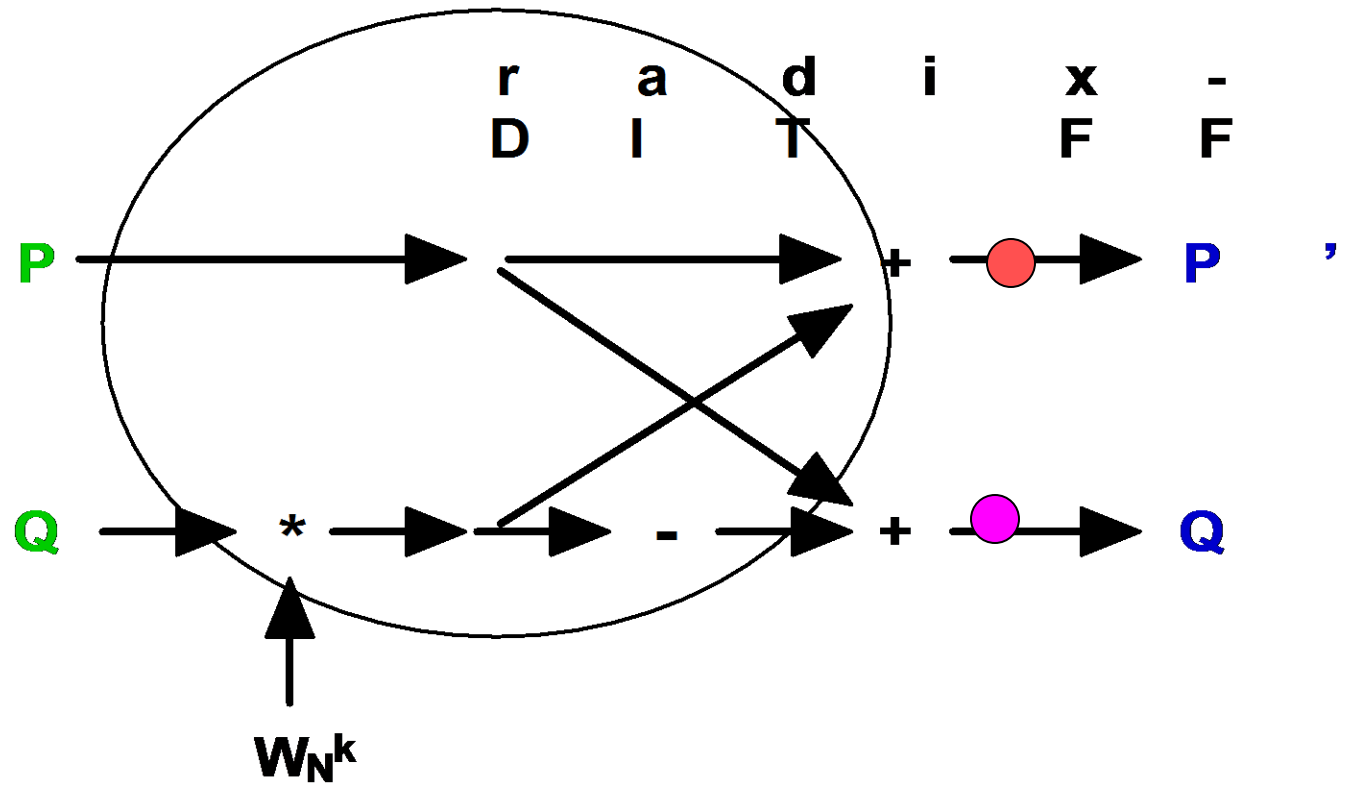
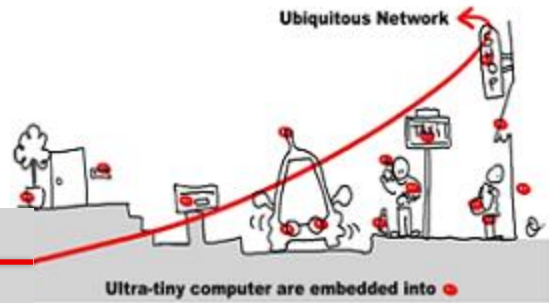
Data Flow



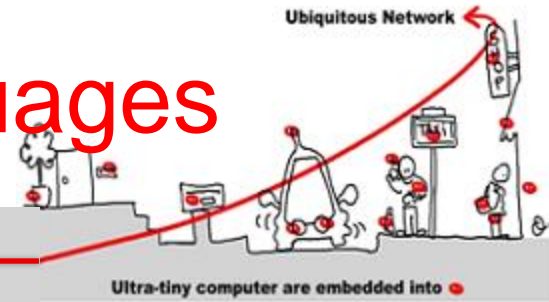
Data Flow



Data Flow

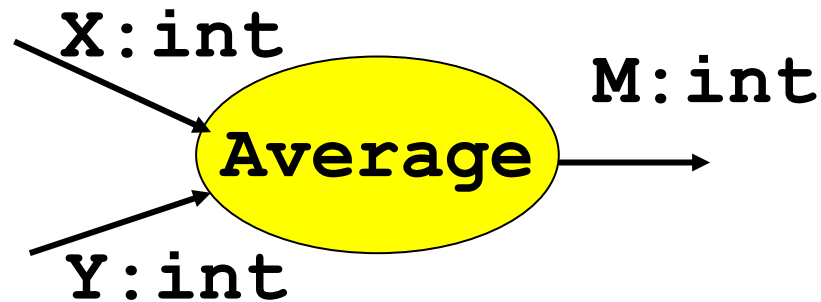
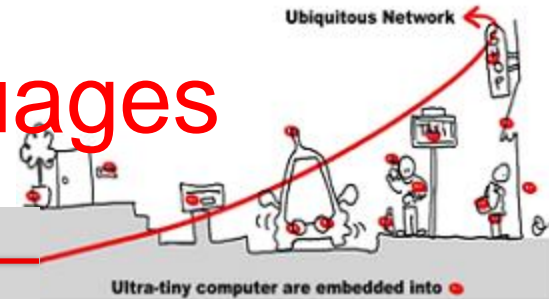


Data Flow Synchronous Languages



1. Data flow programs compute output flows from input flows using:
 1. **Variables** (= flows)
 2. **Equation**: $x = E$ means $\forall k \quad x_k = E_k$
 3. **Assertion**: Boolean expression that should be always true.
2. Data flow programs define new data flow operators.

Data Flow Synchronous Languages



operator **Average** (X,Y:int) returns (M:int)

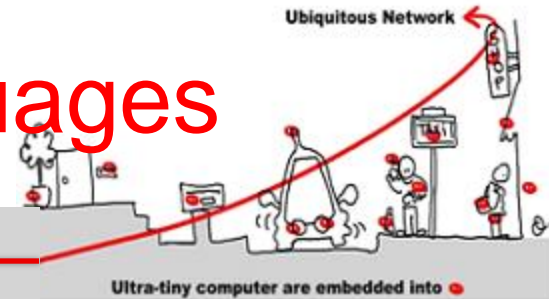
$$M = (X + Y)/2$$

$$X = (X_1, X_2, \dots, X_n, \dots)$$

$$Y = (Y_1, Y_2, \dots, Y_n, \dots)$$

$$M = ((X_1 + Y_1)/2, (X_2 + Y_2)/2, \dots, (X_n + Y_n)/2, \dots)$$

Data Flow Synchronous Languages



Memorizing to take the past into account:

1. **pre (previous):**

$$X = (x_1, x_2, \dots, x_n, \dots) :$$

$$\text{pre}(X) = (\text{nil}, x_1, x_2, \dots, x_n, \dots)$$

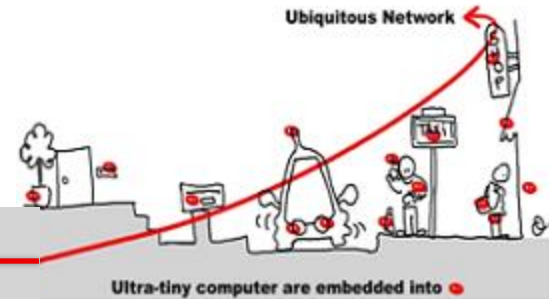
nil undefined value denoting uninitialized memory

2. **→ (initialize):**

$$X = (x_1, x_2, \dots, x_n, \dots), Y = (y_1, y_2, \dots, y_n, \dots) :$$

$$X \rightarrow Y = (x_1, y_2, \dots, y_n, \dots)$$

Sequential examples



$$n = 0 \rightarrow \text{pre}(n) + 1$$

operator **MinMax** ($x:\text{int}$) returns ($\text{min}, \text{max}:\text{int}$):

$\text{min} = x \rightarrow \text{if } (x < \text{pre}(\text{min})) \text{ then } x \text{ else } \text{pre}(\text{min})$

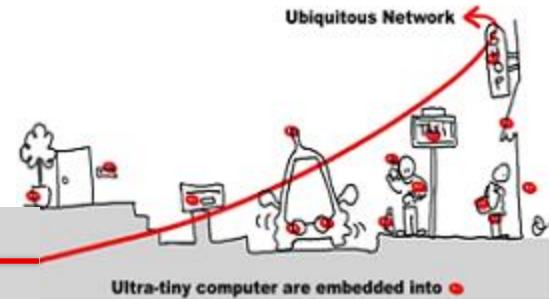
$\text{max} = x \rightarrow \text{if } (x > \text{pre}(\text{max})) \text{ then } x \text{ else } \text{pre}(\text{max})$

$x = (3, 4, 5, 2, 7, \dots)$

$\text{min} = (3, 3, 3, 2, 2, \dots)$

$\text{max} = (3, 4, 5, 5, 7, \dots)$

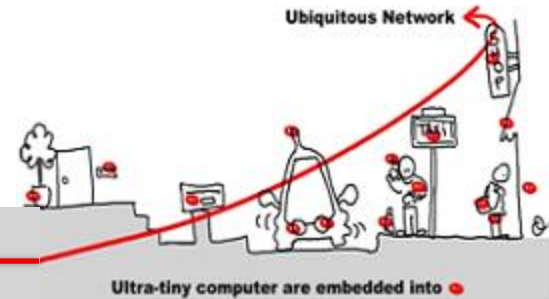
Sequential examples



operator **CT** (init:int) returns (c:int):
 $c = \text{init} \rightarrow \text{pre}(c) + 2$

operator **DoubleCall** (even:bool) returns (n:int)
 $n = \text{if (even) then CT(0) else CT(1)}$
DoubleCall (ff,ff,tt,tt,ff,ff,tt,tt,ff) = ?

Sequential examples



operator **CT** (init:int) returns (c:int):

$$c = \text{init} \rightarrow \text{pre}(c) + 2$$

$$\text{CT}(0) = (0, 2, 4, 6, 8, 10, 12, 14, 16, 18, \dots)$$

$$\text{CT}(1) = (1, 3, 5, 7, 9, 11, 13, 15, 17, 19, \dots)$$

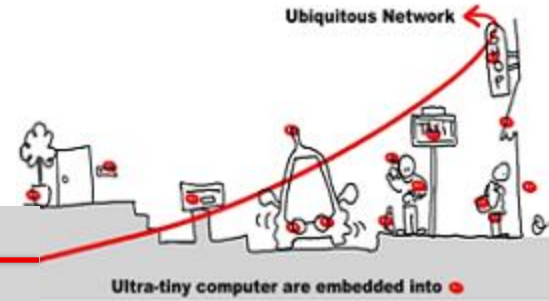
operator **DoubleCall** (even:bool) returns (n:int)

$$n = \text{if (even) then CT}(0) \text{ else CT}(1)$$

$$\text{DoubleCall (ff,ff,tt,tt,ff,ff,tt,tt,ff)} = ?$$

$$(1, 3, 4, 6, 9, 11, 12, 14, 17)$$

Modulo Counter



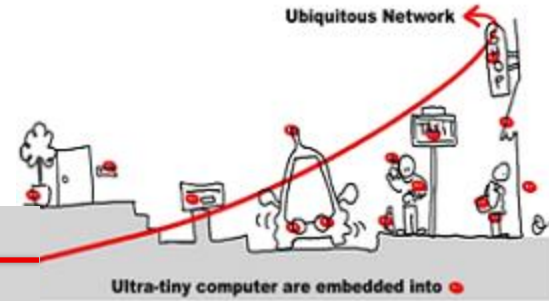
```
operator MCounter (incr:bool; modulo : int)  
    returns (cpt:int);
```

```
var count : int;
```

```
count = 0 -> if incr pre (cpt) + 1  
             else pre (cpt);
```

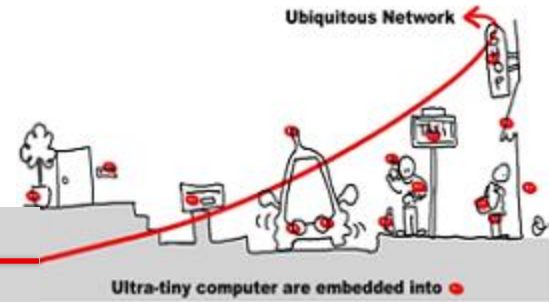
```
cpt = count mod modulo;
```

Modulo Counter Clock



```
operator MCounterClock (incr:bool;  
                        modulo : int)  
    returns(cpt:int;  
           modulo_clock: bool);  
  
var count : int;  
count = 0 -> if incr pre (cpt) + 1  
             else pre (cpt);  
cpt = count mod modulo;  
modulo_clock = count != cpt;
```

Modulo Counter Clock



```
MCounterClock(true,3):
```

```
count:          0 1 2 3 1 2 3.....
```

```
cpt =           0 1 2 0 1 2 0.....
```

```
modulo_clock = ff ff ff tt ff ff tt ...
```

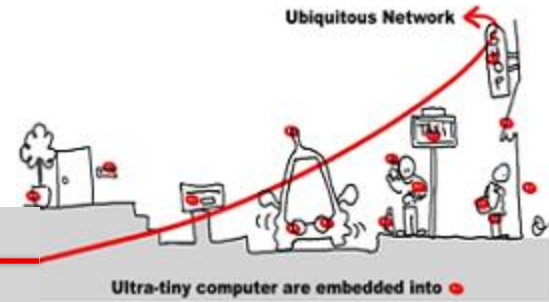
```
var count : int;
```

```
count = 0 -> if incr pre (cpt) + 1  
              else pre (cpt);
```

```
cpt = count mod modulo;
```

```
modulo_clock = count != cpt;
```

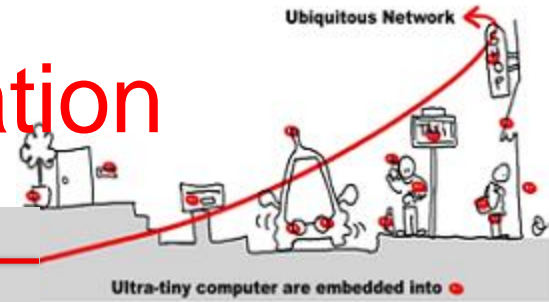

Timer



```
operator Timer returns (hour, minute, second:int);  
var hour_clock, minute_clock, day_clock : bool;
```

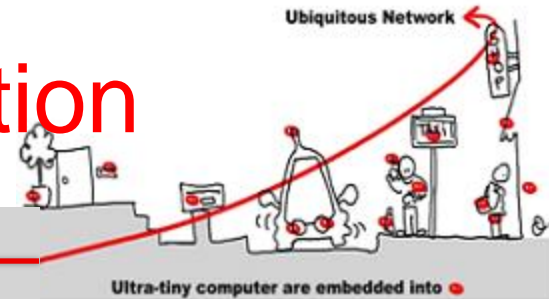
```
(second, minute_clock) = MCounterClock(true, 60);  
(minute, hour_clock) = MCounterClock(minute_clock, 60);  
(hour, dummy_clock) = MCounterClock(hour_clock, 24);
```

Data Flow Programs Compilation



Data flow programs are compiled into automata

Data Flow Program Compilation



operator **WD** (set, reset, deadline:bool)
returns (alarm:bool);

var is_set:bool;

alarm = is_set and deadline;

is_set = false -> if set then true

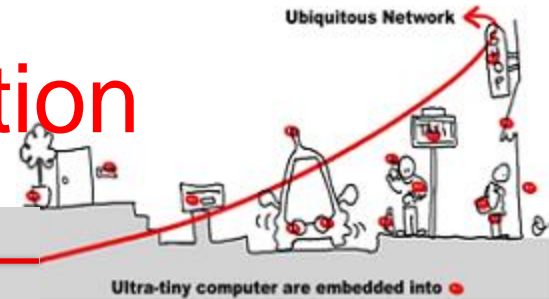
else if reset then false

else **pre**(is_set);

assert not(set and reset);

tel.

Data Flow Program Compilation



First, the program is translated into pseudo code:

```
if _init then // first instant (or reaction)
```

```
  is_set := false; alarm := false;
```

```
  _init := false;
```

```
else // following reactions
```

```
  if set then is_set := true
```

```
  else
```

```
    if reset then is_set := false;
```

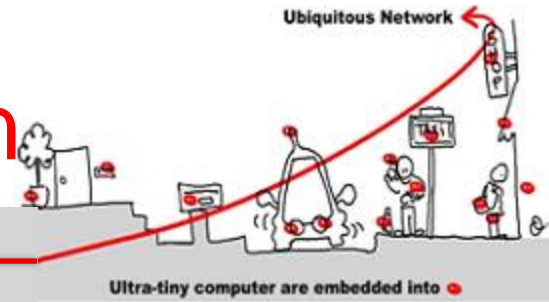
```
    endif
```

```
  endif
```

```
  alarm := is_set and deadline;
```

```
endif
```

Data Flow Program Compilation



Choose state variables : **_init** and variables which have **pre**.

For WD, we consider 2 state variables:

_init (true, false, false, ...) and **pre(is_set)**

3 states:

S0: **_init** = true and **pre(is_set)** = nil

S1: **_init** = false and **pre(is_set)** = false

S2: **_init** = false and **pre(is_set)** = true

Data Flow Program Compilation

Ubiquitous Network

Ultra-tiny computer are embedded into

initial

S0: alarm := false;

S1:

_init := false
pre(is_set) := false

```
if _init then // first instant (or
reaction)
  is_set := false; alarm := false;
  _init := false;
else // following reactions
  if set then is_set := true
  else
    if reset then is_set := false;
  endif
endif
alarm := is_set and deadline;
endif
```

Lustre Program Compilation



initial

S0: alarm := false;

```
S1: if set then
  alarm := deadline;
  go to S2;
else
  alarm := false;
  go to S1;
```

set

\neg set

```
if _init then // first instant (or
reaction)
  is_set := false; alarm := false;
  _init := false;
else // following reactions
  if set then is_set := true
  else
    if reset then is_set := false;
  endif
endif
alarm := is_set and deadline;
endif
```

Lustre Program Compilation

Ubiquitous Network

Ultra-tiny computer are embedded into

initial

S0: alarm := false;

S1: if set then
 alarm := deadline;
 go to S2;
else
 alarm := false;
 go to S1;

set

S2:

_init = false;
pre(is_set) := true;

¬set

Lustre Program Compilation

Ubiquitous Network

Ultra-tiny computer are embedded into

initial

S0: alarm := false;

```
if _init then // first instant (or reaction)
  is_set := false; alarm := false;
  _init := false;
else // following reactions
  if set then is_set := true
  else
    if reset then is_set := false;
  endif
endif
alarm := is_set and deadline;
endif
```

set

reset

```
S2: if set then
  alarm := deadline;
  go to S2;
else
  if reset then
    alarm := false;
    go to S1;
  else
    alarm := deadline;
    go to S2;
  endif
endif
```

-reset

Lustre Program Compilation

Ubiquitous Network

Ultra-tiny computer are embedded into

initial

S0: alarm := false;

S1: if set then
 alarm := deadline;
 go to S2;
else
 alarm := false;
 go to S1;

set

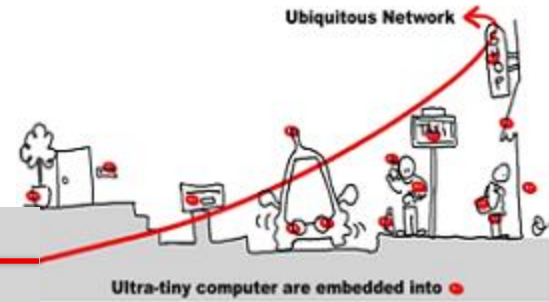
S2: if set then
 alarm := deadline;
 go to S2;
else
 if reset then
 alarm := false;
 go to S1;
 else
 alarm := deadline;
 go to S2;

reset

\neg set

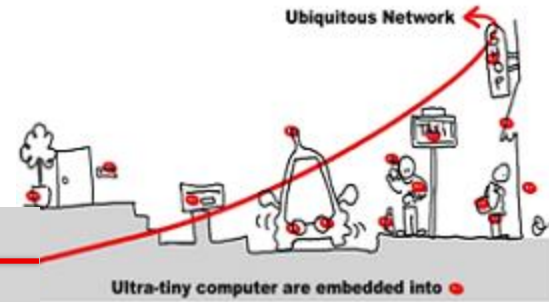
\neg reset

Model Checking Technique



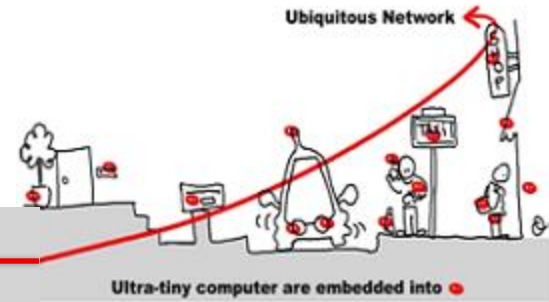
- Model = automata which is the set of program behaviors
- Properties expression = temporal logic:
 - LTL : liveness properties
 - CTL: safety properties
- Algorithm =
 - LTL : algorithm exponential wrt the formula size and linear wrt automata size.
 - CTL: algorithm linear wrt formula size and wrt automata size

Properties Checking



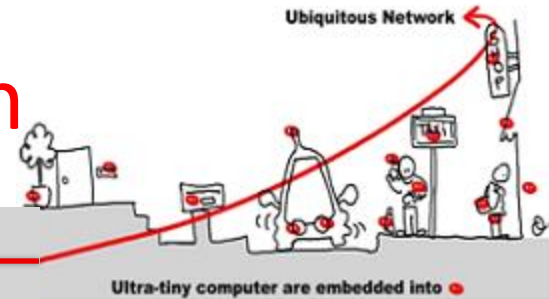
- Liveness Property Φ :
 - $\Phi \Rightarrow$ automata $B(\Phi)$
 - $L(B(\Phi)) = \emptyset$ decidable
 - $\Phi \models \mathcal{M} : L(\mathcal{M} \otimes B(\sim\Phi)) = \emptyset$

Safety Properties



- CTL formula characterization:
 - Atomic formulas
 - Usual logic operators: not, and, or (\Rightarrow)
 - Specific temporal operators:
 - $EX \ \emptyset$, $EF \ \emptyset$, $EG \ \emptyset$
 - $AX \ \emptyset$, $AF \ \emptyset$, $AG \ \emptyset$
 - $EU(\emptyset_1, \emptyset_2)$, $AU(\emptyset_1, \emptyset_2)$

Safety Properties Verification



We call $\text{Sat}(\emptyset)$ the set of states where \emptyset is true.

$\mathcal{M} \models \emptyset$ iff $s_{\text{init}} \in \text{Sat}(\emptyset)$.

Algorithm:

$$\text{Sat}(\Phi) = \{s \mid \Phi \models s\}$$

$$\text{Sat}(\text{not } \Phi) = S \setminus \text{Sat}(\Phi)$$

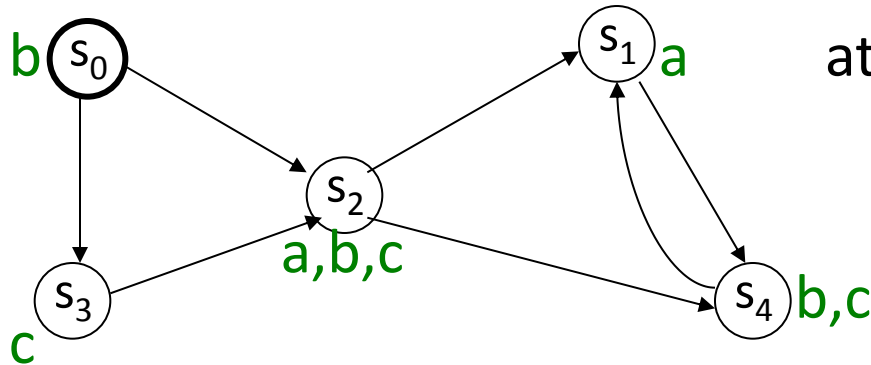
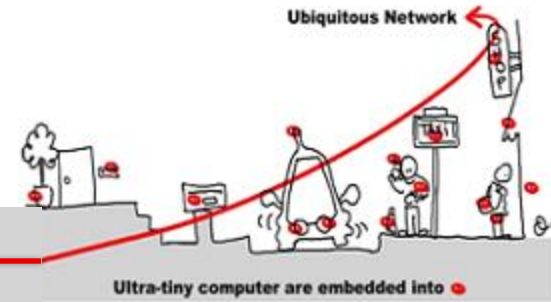
$$\text{Sat}(\Phi_1 \text{ or } \Phi_2) = \text{Sat}(\Phi_1) \cup \text{Sat}(\Phi_2)$$

$$\text{Sat}(\text{EX } \Phi) = \{s \mid \exists t \in \text{Sat}(\Phi), s \rightarrow t\} \quad (\text{Pre } \text{Sat}(\Phi))$$

$$\text{Sat}(\text{EG } \Phi) = \text{gfp } (\Gamma(x) = \text{Sat}(\Phi) \cap \text{Pre}(x))$$

$$\text{Sat}(\text{E}(\Phi_1 \cup \Phi_2)) = \text{lfp } (\Gamma(x) = \text{Sat}(\Phi_2) \cup (\text{Sat}(\Phi_1) \cap \text{Pre}(x)))$$

Example



atomic formulas: a, b, c

EG (a or b)

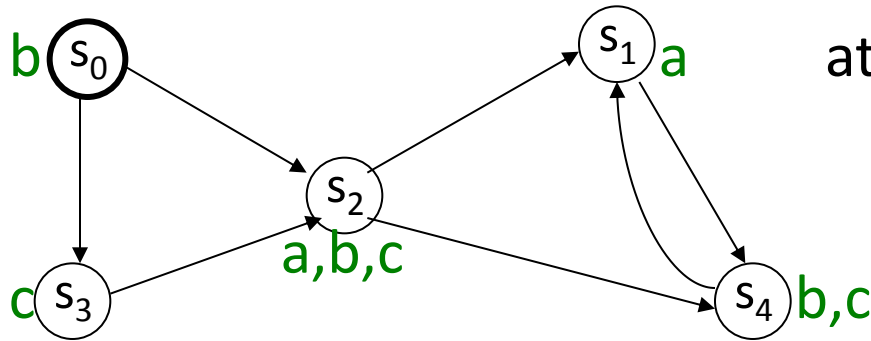
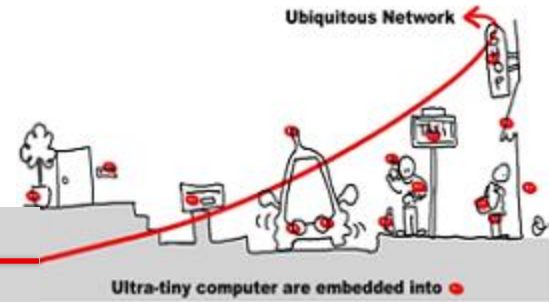
$gfp (\Gamma(x) = \text{Sat}(a \text{ or } b) \cap \text{Pre}(x))$

$$\Gamma(\{s_0, s_1, s_2, s_3, s_4\}) = \text{Sat}(a \text{ or } b) \cap \text{Pre}(\{s_0, s_1, s_2, s_3, s_4\})$$

$$\Gamma(\{s_0, s_1, s_2, s_3, s_4\}) = \{s_0, s_1, s_2, s_4\} \cap \{s_0, s_1, s_2, s_3, s_4\}$$

$$\Gamma(\{s_0, s_1, s_2, s_3, s_4\}) = \{s_0, s_1, s_2, s_4\}$$

Example



atomic formulas: a, b, c

EG (a or b)

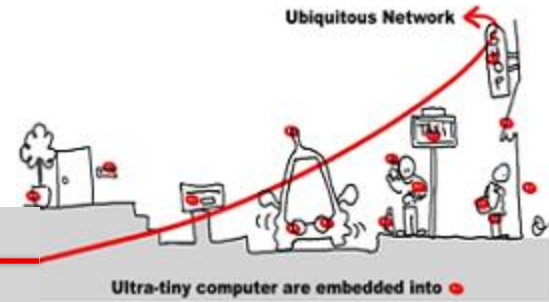
$$\Gamma(\{s_0, s_1, s_2, s_3, s_4\}) = \{s_0, s_1, s_2, s_4\}$$

$$\Gamma(\{s_0, s_1, s_2, s_4\}) = \text{Sat}(a \text{ or } b) \cap \text{Pre}(\{s_0, s_1, s_2, s_4\})$$

$$\Gamma(\{s_0, s_1, s_2, s_4\}) = \{s_0, s_1, s_2, s_4\}$$

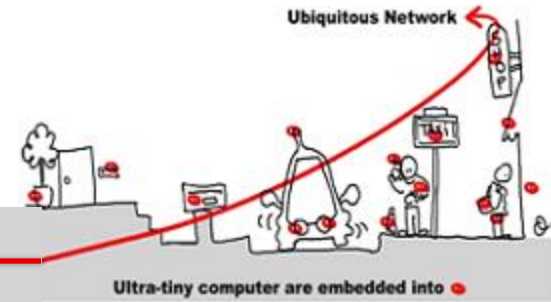
$$s_0 \models \text{EG}(a \text{ or } b)$$

Model Checking Implementation

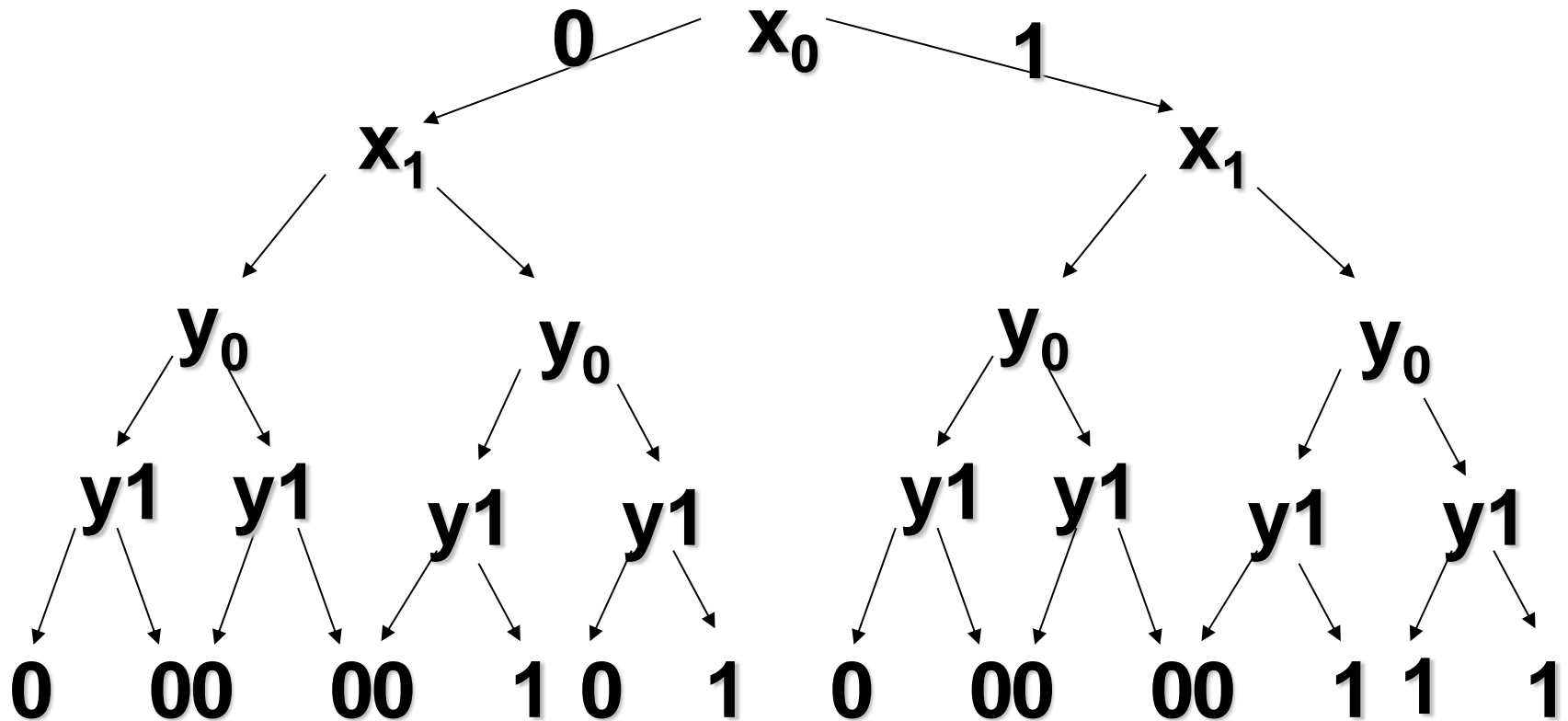


- Problem: the size of automata
- Solution: **symbolic** model checking
- Usage of BDD (Binary Decision Diagram) to encode both automata and formula.
- Each Boolean function has a **unique** representation
- Shannon decomposition:
 - $f(x_0, x_1, \dots, x_n) = f(1, x_1, \dots, x_n) \vee f(0, x_1, \dots, x_n)$

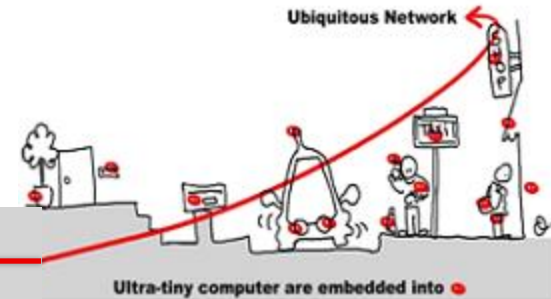
Model Checking Implementation (2)



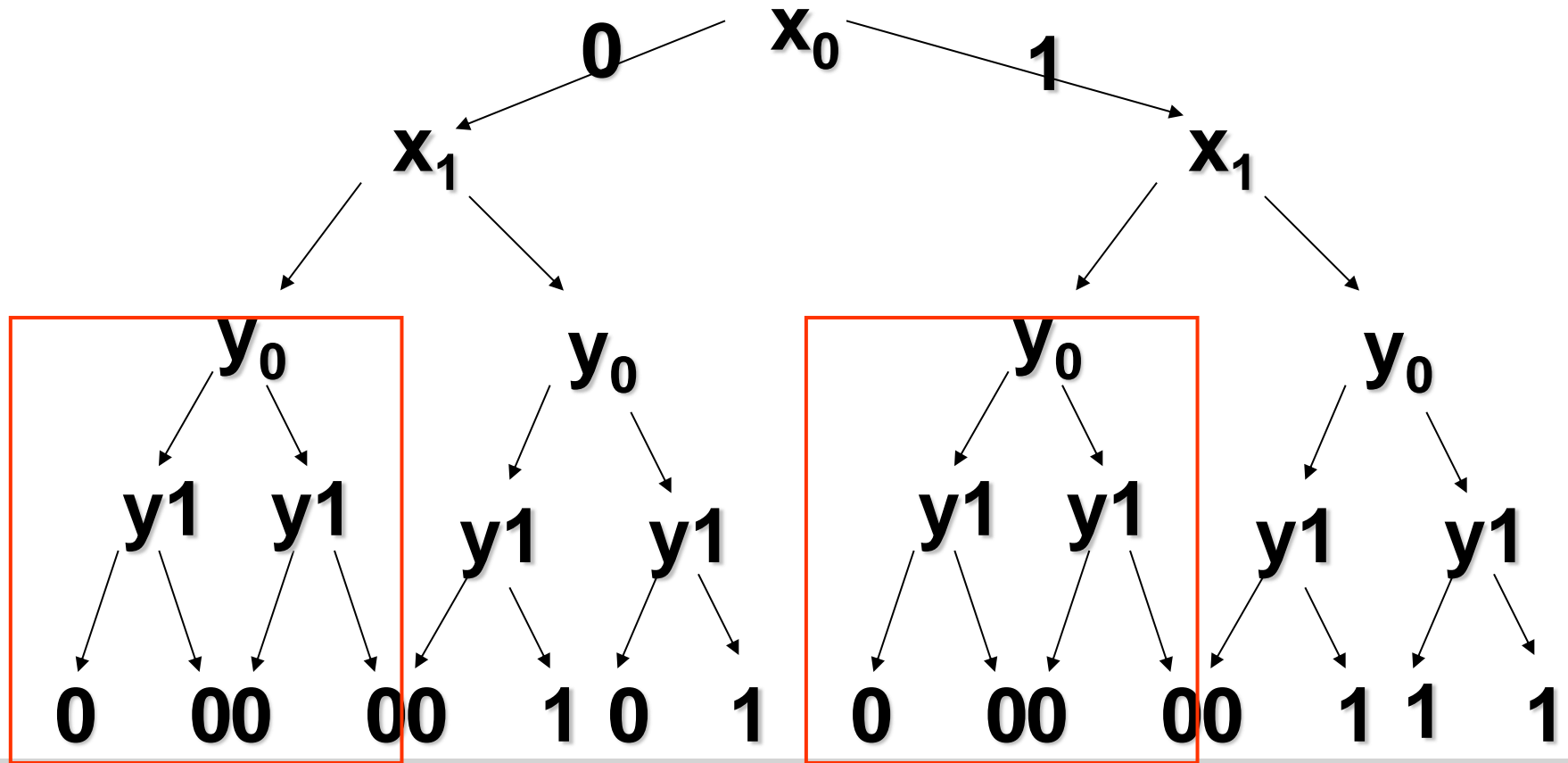
$$(x_1 \wedge y_1) \vee (x_0 \wedge y_0 \wedge x_1)$$



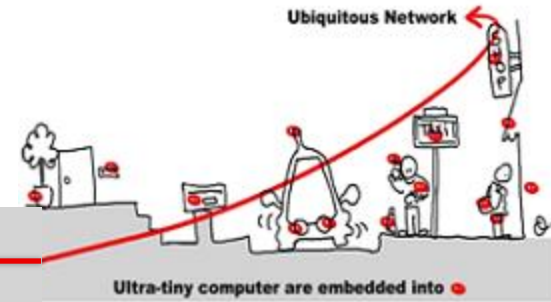
Model Checking Implementation (2)



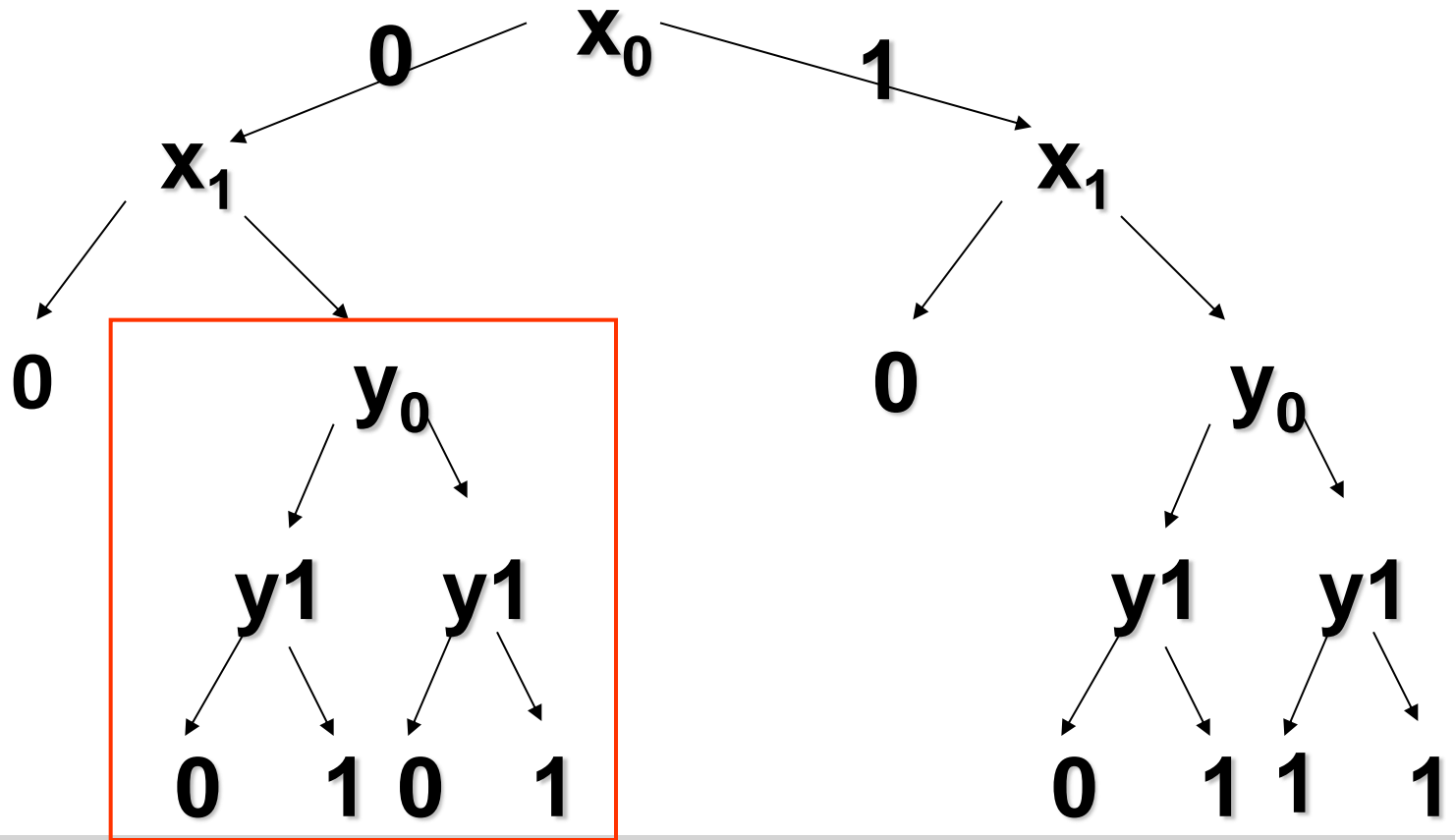
$$(x_1 \wedge y_1) \vee (x_0 \wedge y_0 \wedge x_1)$$



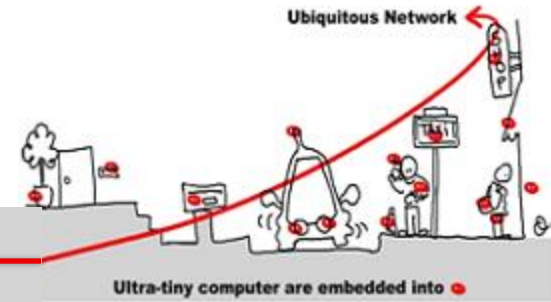
Model Checking Implementation (2)



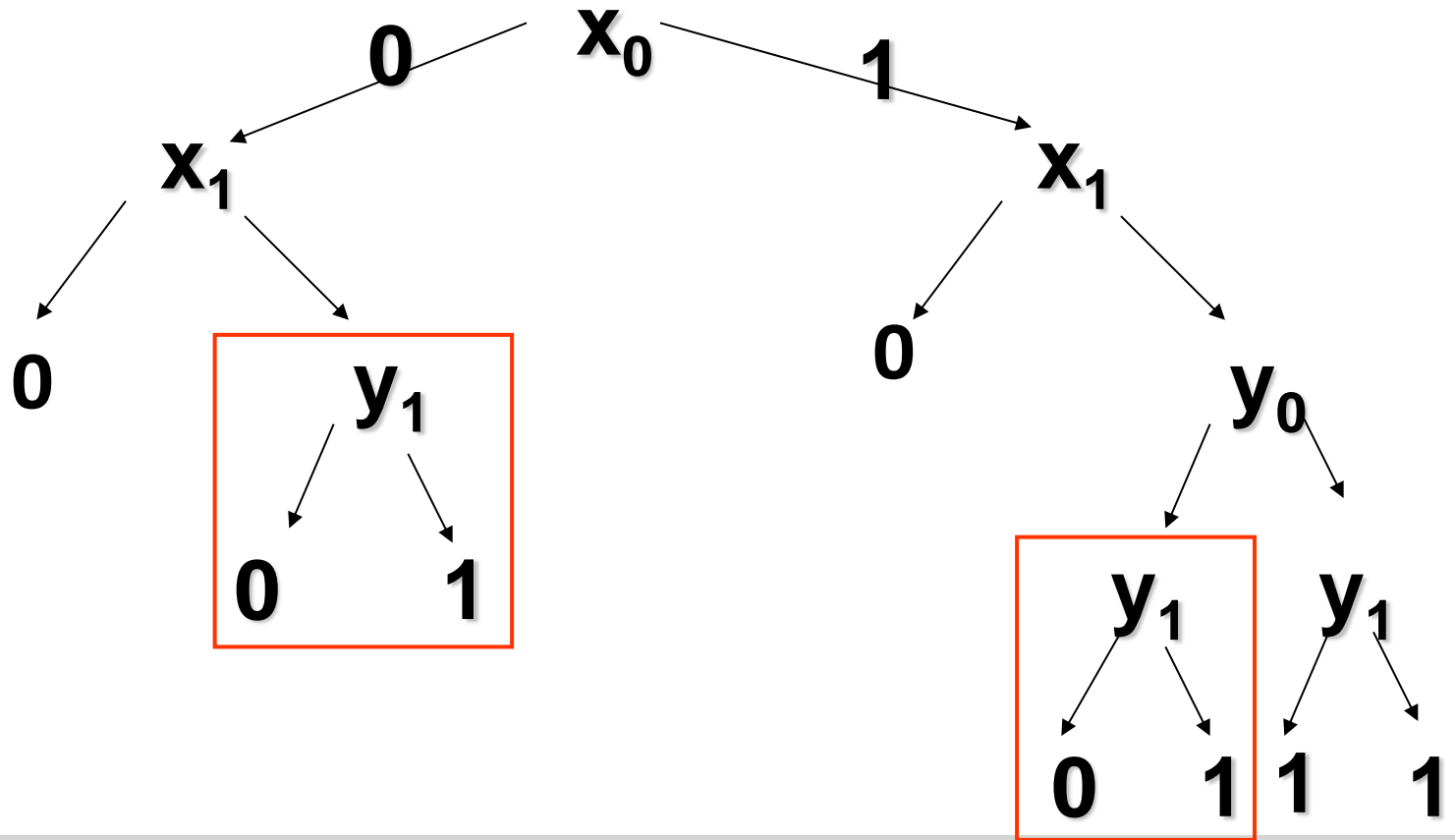
$$(x_1 \wedge y_1) \vee (x_0 \wedge y_0 \wedge x_1)$$



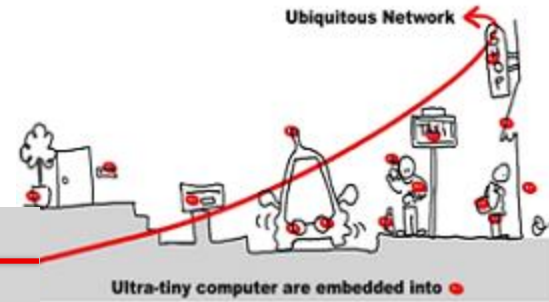
Model Checking Implementation (2)



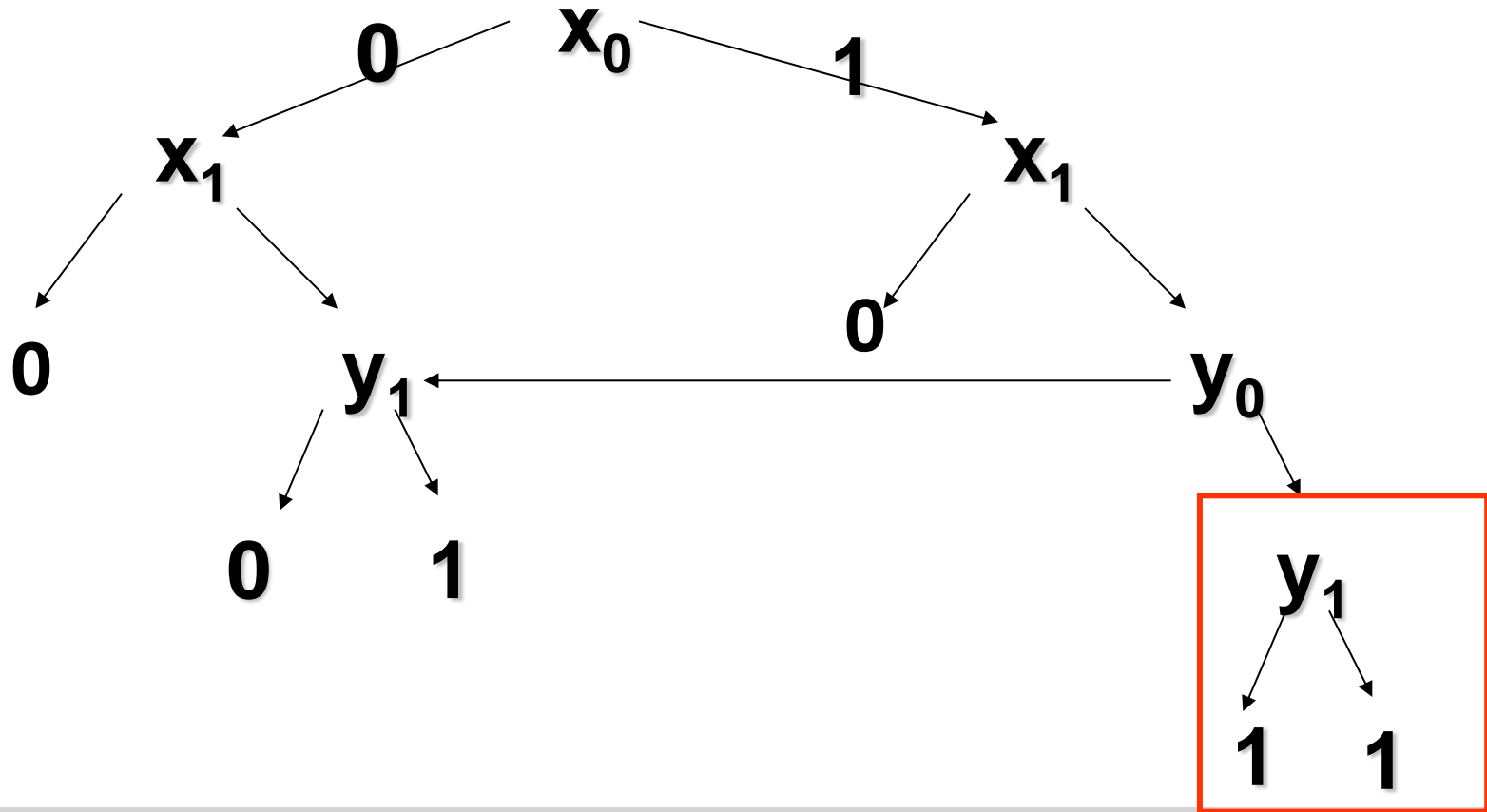
$$(x_1 \wedge y_1) \vee (x_0 \wedge y_0 \wedge x_1)$$



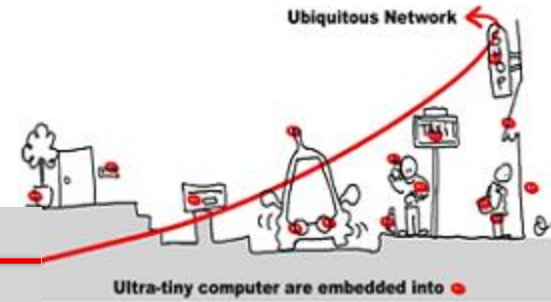
Model Checking Implementation (2)



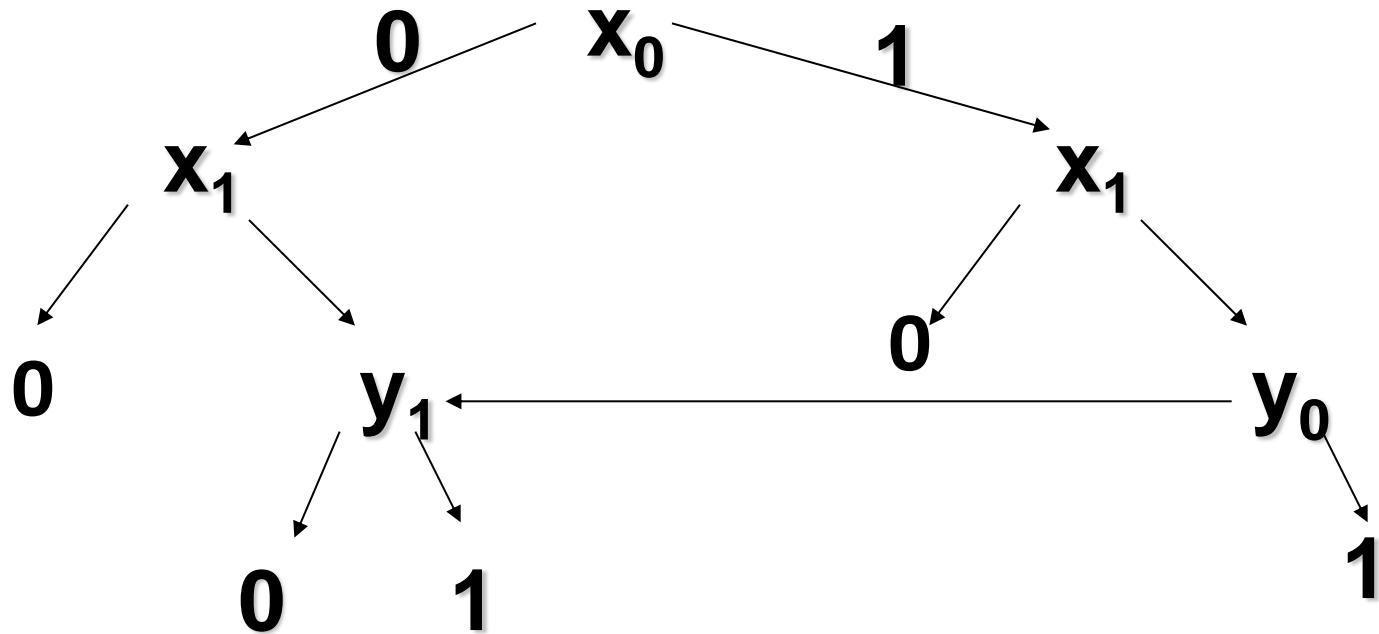
$$(x_1 \wedge y_1) \vee (x_0 \wedge y_0 \wedge x_1)$$



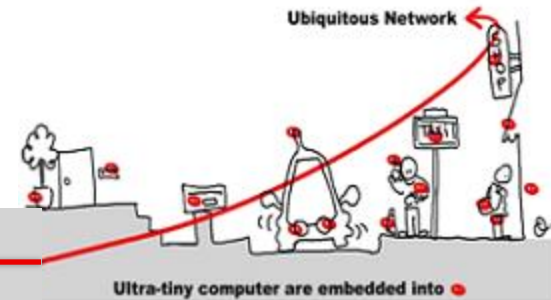
Model Checking Implementation (2)



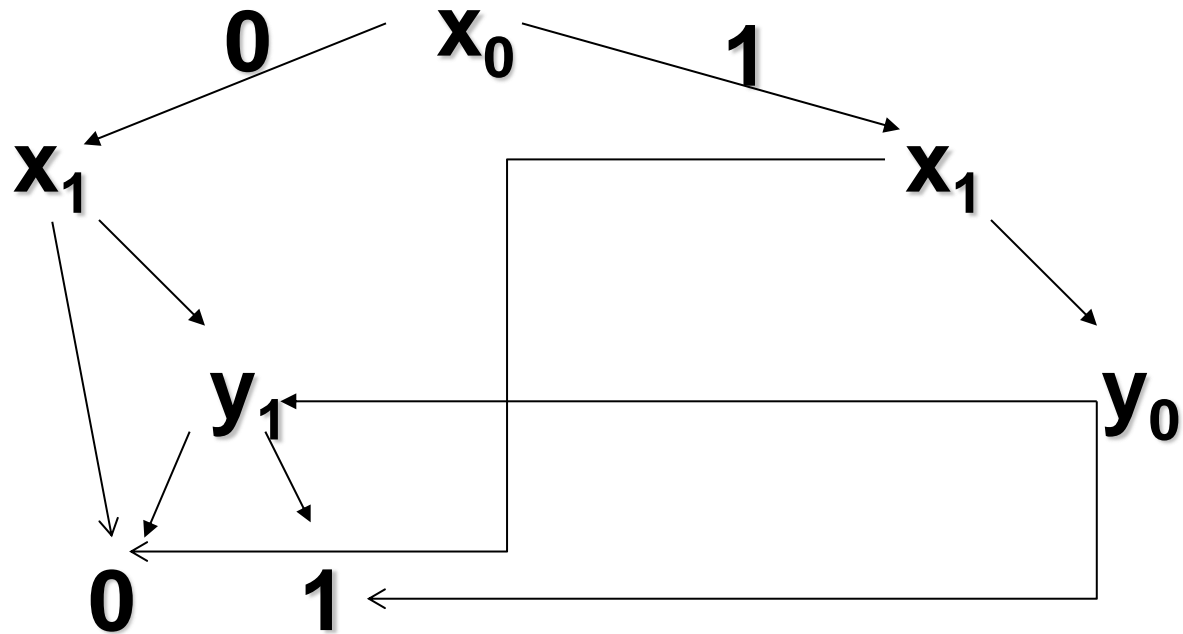
$$(x_1 \wedge y_1) \vee (x_0 \wedge y_0 \wedge x_1)$$



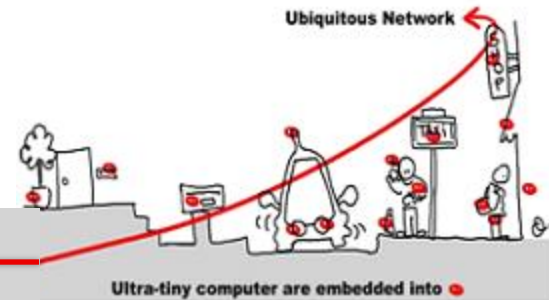
Model Checking Implementation (2)



$$(x_1 \wedge y_1) \vee (x_0 \wedge y_0 \wedge x_1)$$

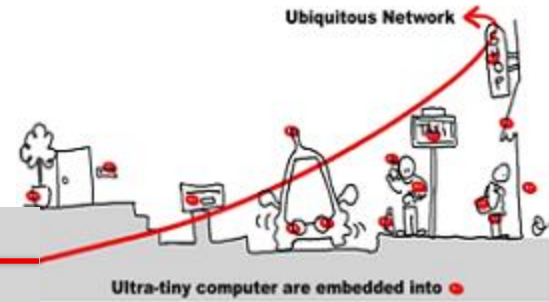


Model Checking Implementation(3)



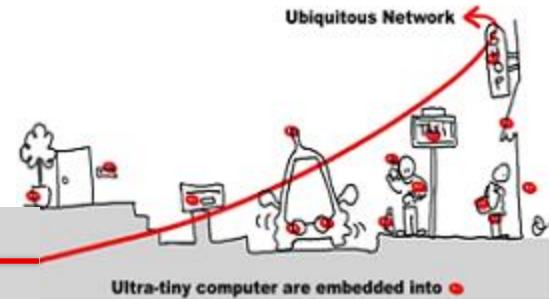
- Implicit representation of the of states set and of the transition relation of automata with BDD.
- BDD allows
 - canonical representation
 - test of emptiness immediate ($bdd = 0$)
 - complementarity immediate ($1 = 0$)
 - union and intersection not immediate
 - Pre immediate

Model Checking Implementation (4)



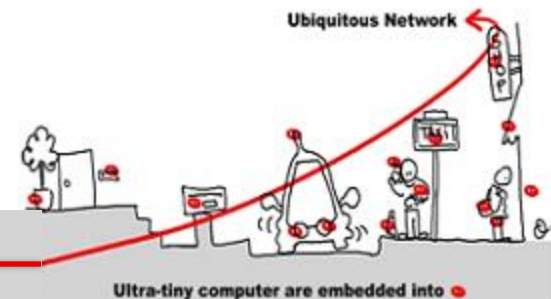
- But BDD efficiency depends on the number of variables
- Other method: **SAT-Solver**
 - Sat-solvers answer the question: given a propositional formula, is there exist a valuation of the formula variables such that this formula holds
 - first algorithm (DPLL) exponential (1960)

Model Checking Implementation (4)



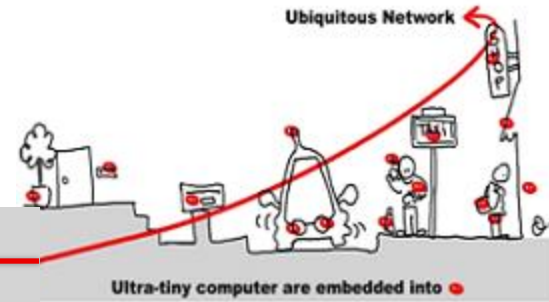
- SAT-Solver algorithm:
 - formula \rightarrow CNF formula \rightarrow set of clauses
 - heuristics to choose variables
 - deduction engine:
 - propagation
 - specific reduction rule application (unit clause)
 - Others reduction rules
 - conflict analysis + learning

Model Checking Implementation (5)



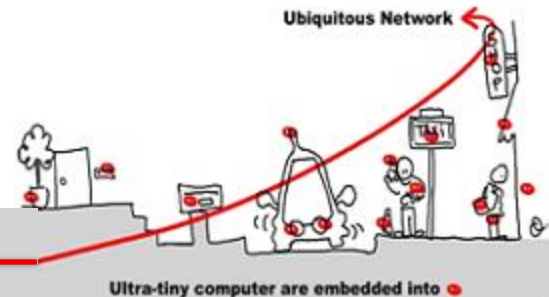
- SAT-Solver usage:
 - encoding of the paths of length k by propositional formulas
 - the existence of a path of length k (for a given k) where a temporal property Φ is true can be reduce to the satisfaction of a propositional formula
 - theorem: given Φ a temporal property and \mathcal{M} a model, then $\mathcal{M} \models \Phi \Rightarrow \exists n$ such that $\mathcal{M} \models_n \Phi$ ($n < |S| \cdot 2^{|\Phi|}$)

Bounded Model Checking

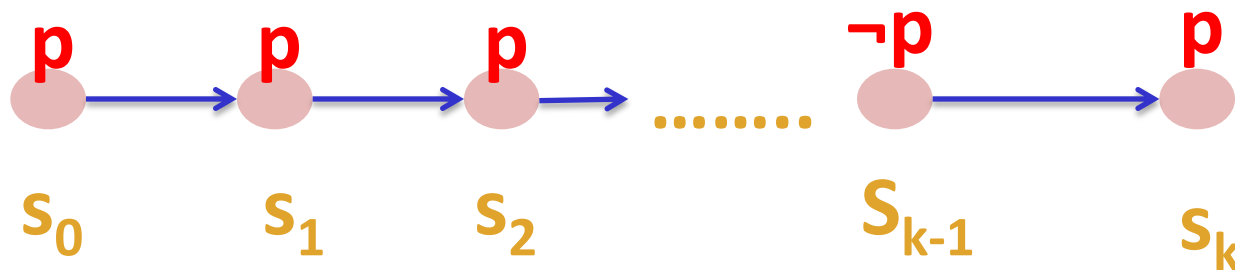


- SAT-Solver are used in complement of implicit (BDD based) methods.
- $\mathcal{M} \models \Phi$
 - verify $\neg \Phi$ on all paths of length k (k bounded)
 - useful to quickly extract counter examples

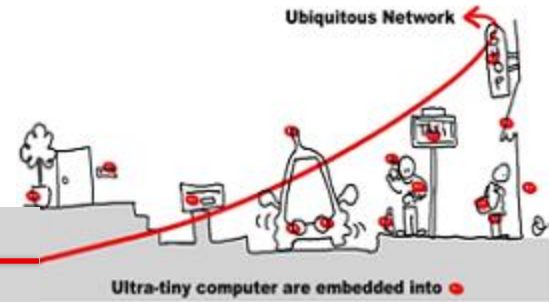
Bounded Model Checking



Given a property p
Is there a state reachable in k steps, which satisfies $\neg p$?



Bounded Model Checking



The reachable states in k steps are captured by:

$$I(s_0) \wedge T(s_0, s_1) \wedge \dots \wedge T(s_{k-1}, s_k)$$

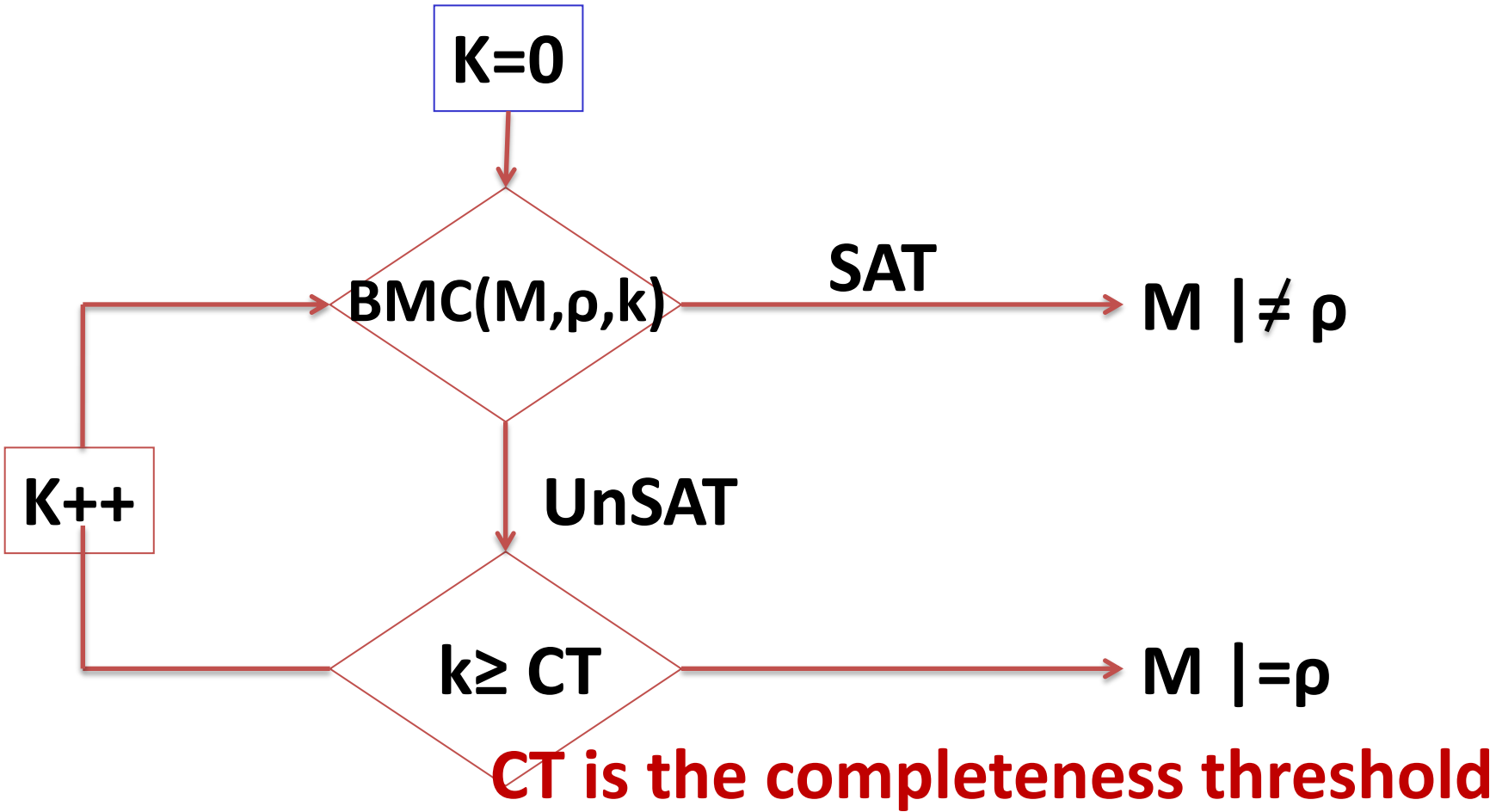
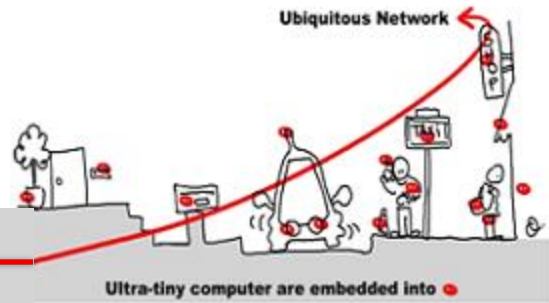
The property p fails in one of the k steps

$$\neg p(s_0) \vee \neg p(s_1) \vee \neg p(s_2) \dots \vee \neg p(s_{k-1}) \vee \neg p(s_k)$$

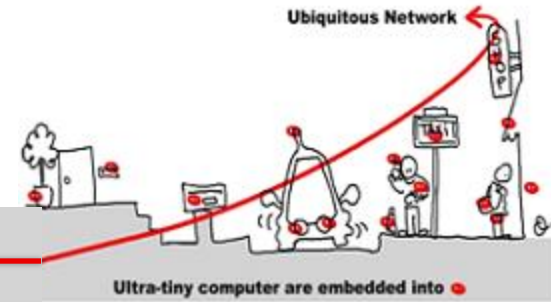
The safety property p is valid up to step k iff $\Omega(k)$ is unsatisfiable:

$$\Omega(k) = I(s_0) \wedge \left(\bigwedge_{i=0}^{k-1} T(s_i, s_{i+1}) \right) \wedge \left(\bigvee_{i=0}^k \neg p(s_i) \right)$$

Bounded Model Checking

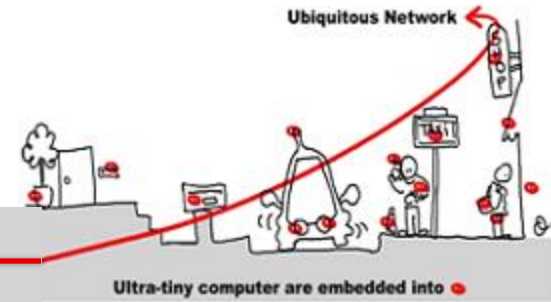


Bounded Model Checking

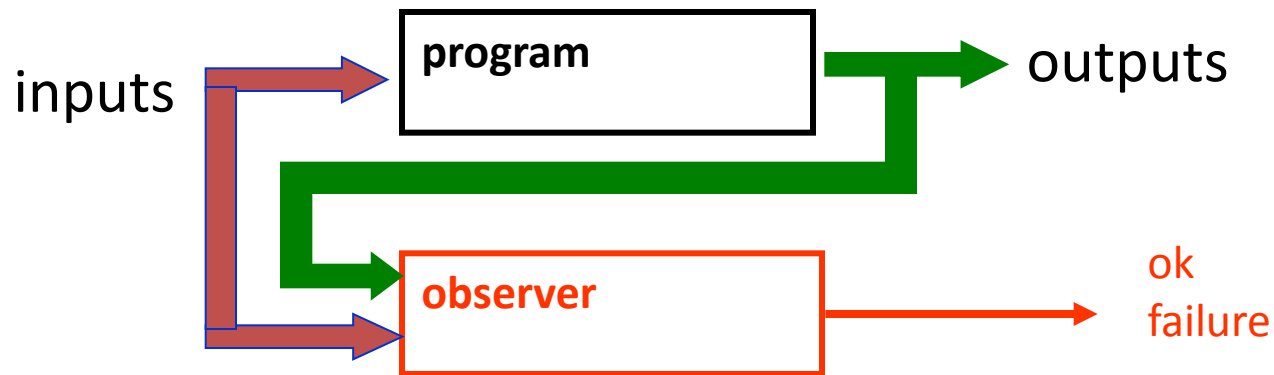


- Computing CT is **as hard as model checking**.
- Idea: Compute an over-approximation to the actual CT
 - Consider the system *as a graph*.
 - Compute *CT from structure of the graph*.
- Example: for **AGp** properties, CT is the longest shortest path between any two reachable states, starting from initial state

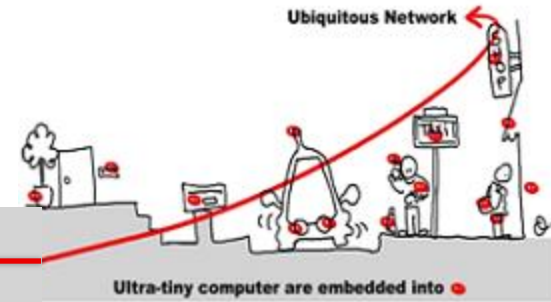
Model Checking with Observers



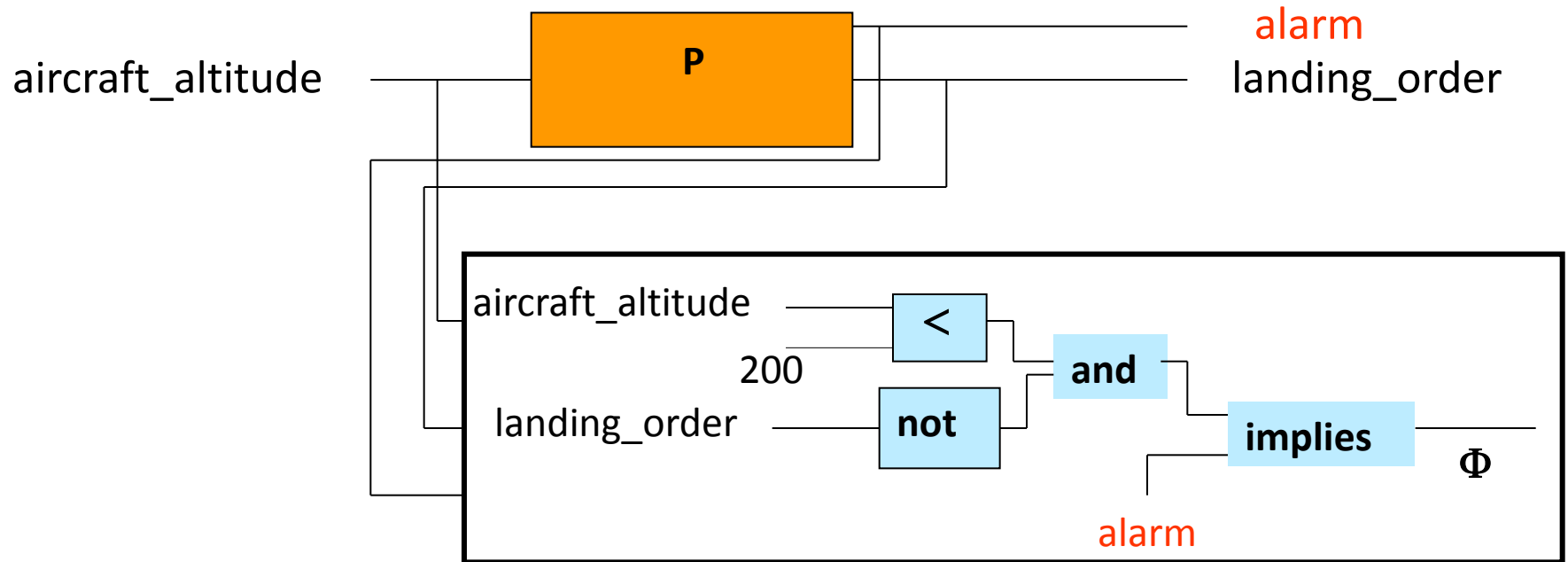
- Express safety properties as **observers**.
- An observer is a program which observes the program and outputs **ok** when the property holds and **failure** when its fails



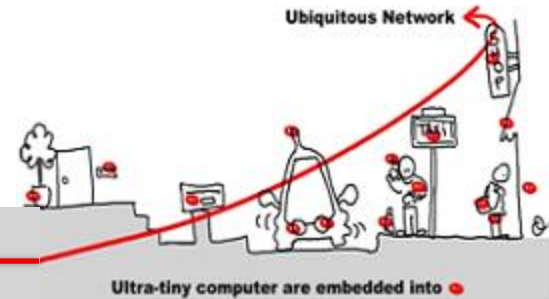
Model Checking with observers (2)



P: aircraft autopilot and security system

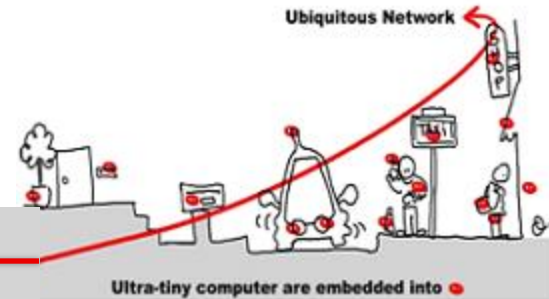


Properties Validation

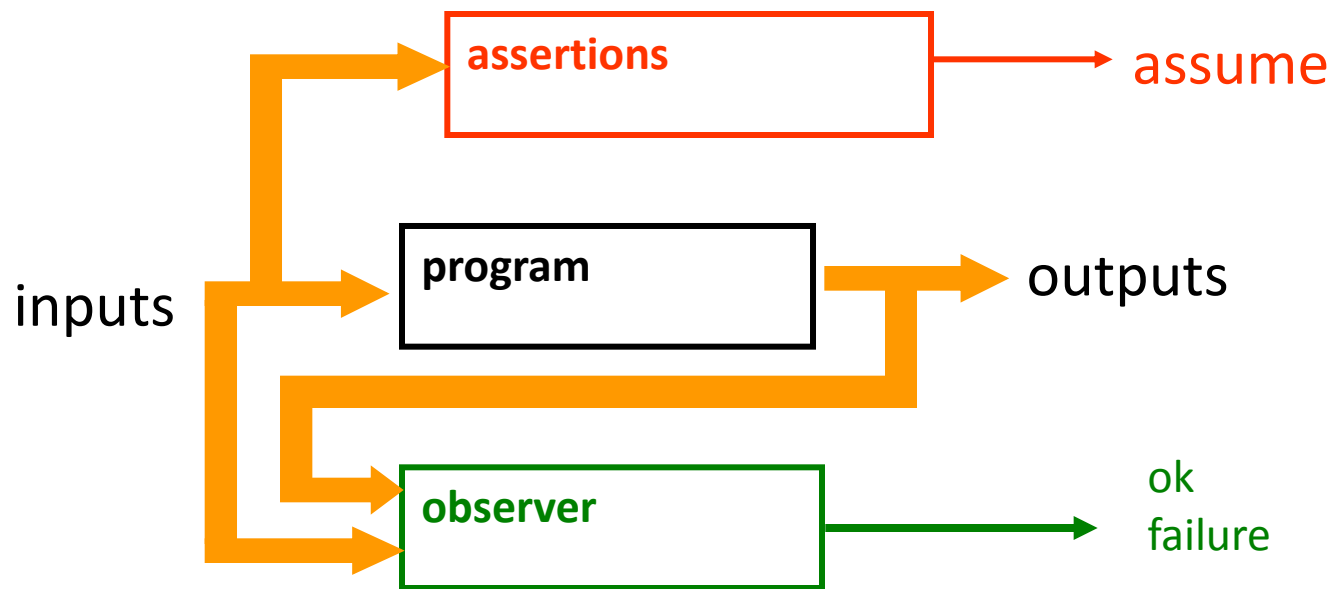


- Taking into account the **environment**
 - without any assumption on the environment, proving properties is difficult
 - but the environment is **indeterminist**
 - Human presence no predictable
 - Fault occurrence
 - ...
 - Solution: use assertion to make **hypothesis** on the environment and make it determinist

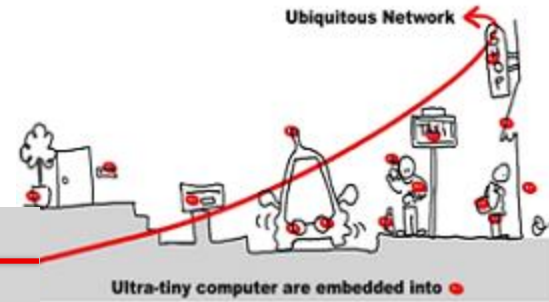
Properties Validation (2)



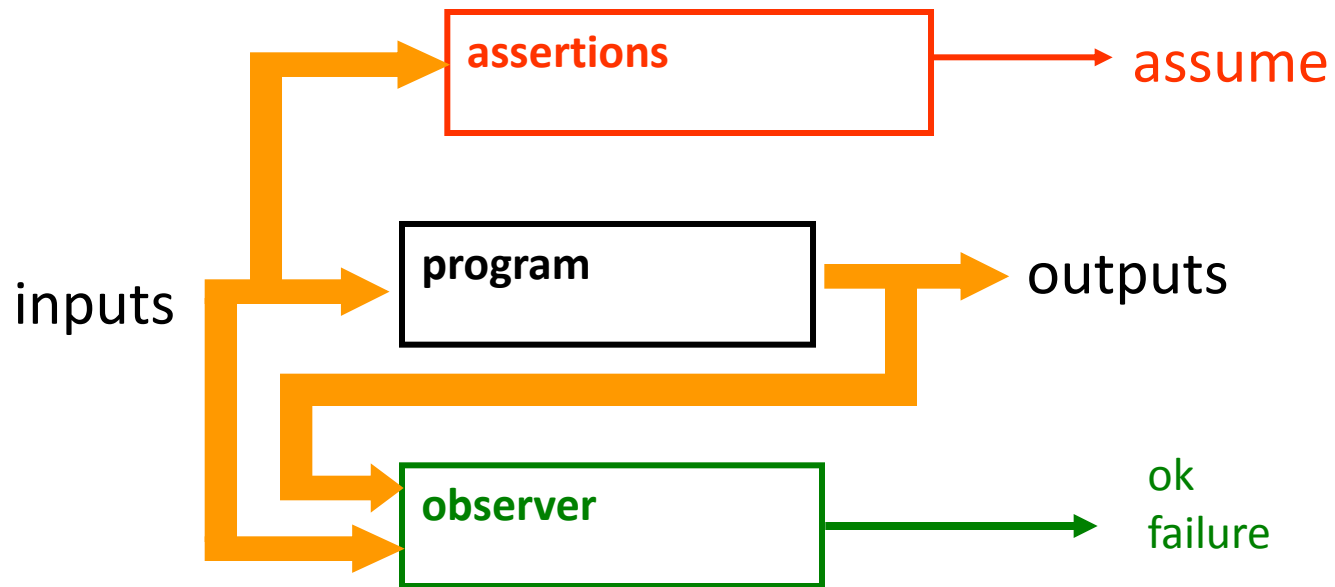
- Express safety properties as **observers**.
- Express constraints about the environment as **assertions**.



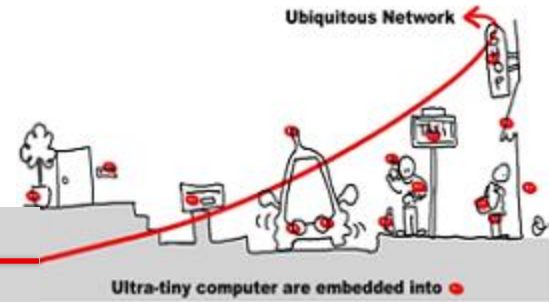
Properties Validation (3)



- if **assume** remains true, then **ok** also remains true (or failure false).

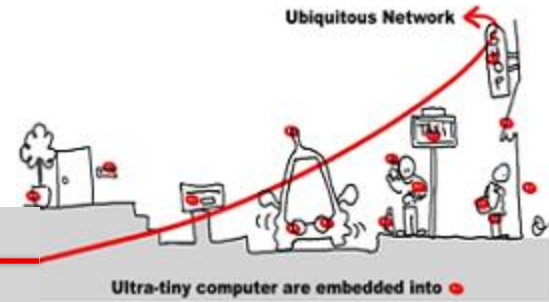


Outline



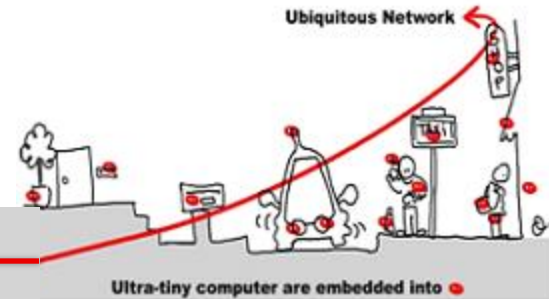
1. Critical system validation
2. Model-checking solution
 1. Model specification
 2. Model-checking techniques
3. Application to component based adaptive middleware
 1. Middleware critical component as synchronous models to allow validation
 2. The **Scade** solution

Practical Issues



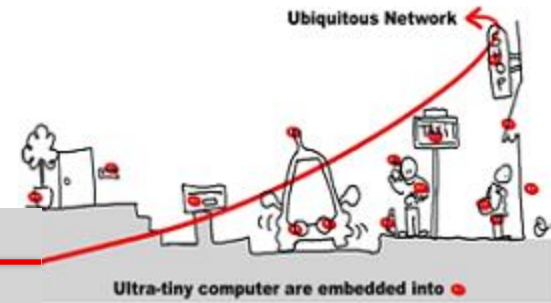
Application to Component Based
Adaptive Middleware for
Ubiquitous Computing

Component Modeling



- Adaptive middleware (as Wcomp) component listen to input events and provide output methods in reaction.
- They could be critical and response time sensitive
 - They should support **formal validation**
 - They should be **deterministic**
- Component behavior specification as **synchronous model**

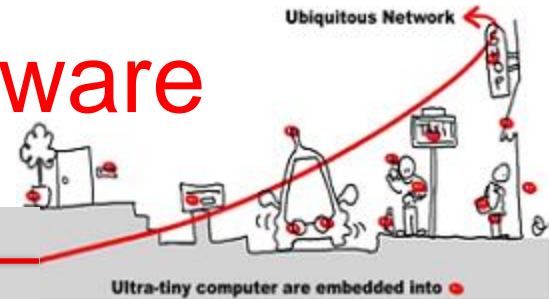
Synchronous Models



To sum up :

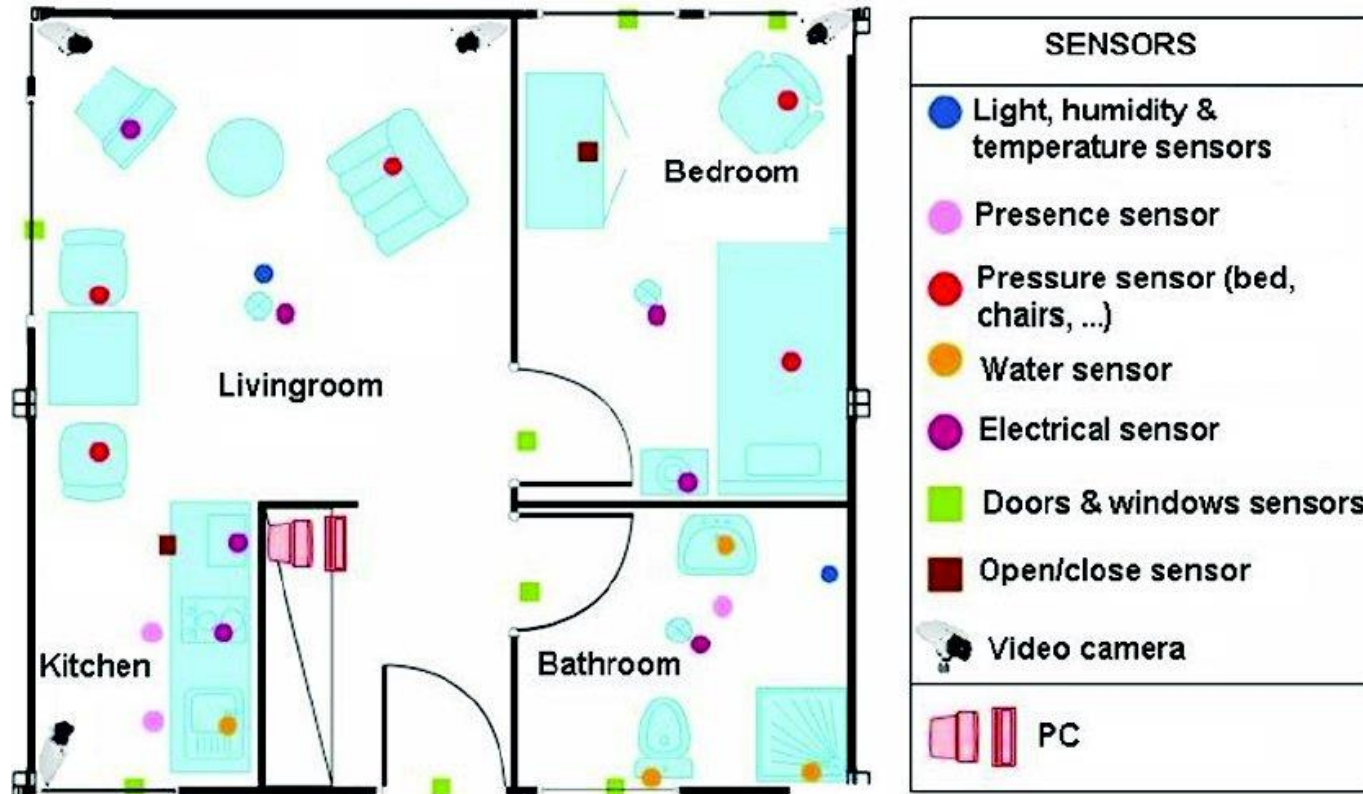
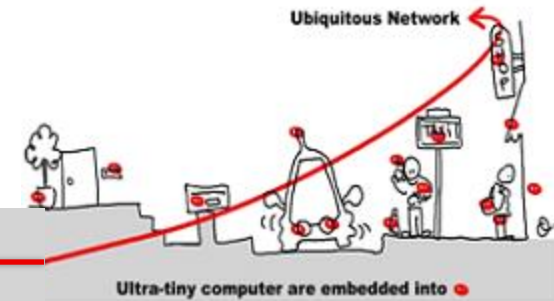
1. Synchronous models can be designed as **event-driven controllers** or as **data flow operator networks**
2. They always represent automata
3. Model-checking techniques apply

Application to Adaptive Middleware



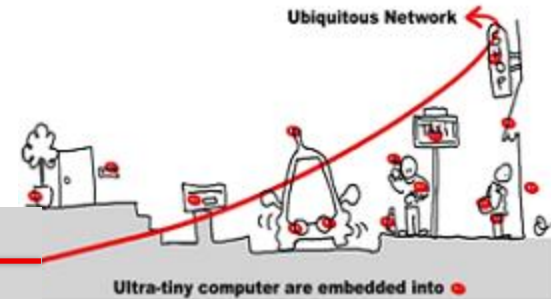
- Our goal is to validate critical component of component based adaptive middleware for ubiquitous computing
- **critical component** will provide a **synchronous model** of their behaviors to allow model-checking techniques application as validation
- This synchronous model will be translated into a specific component called a **synchronous monitor**

Use Case



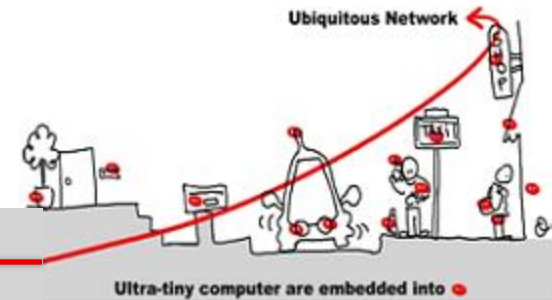
Old adults monitoring in an instrumented home

Use Case

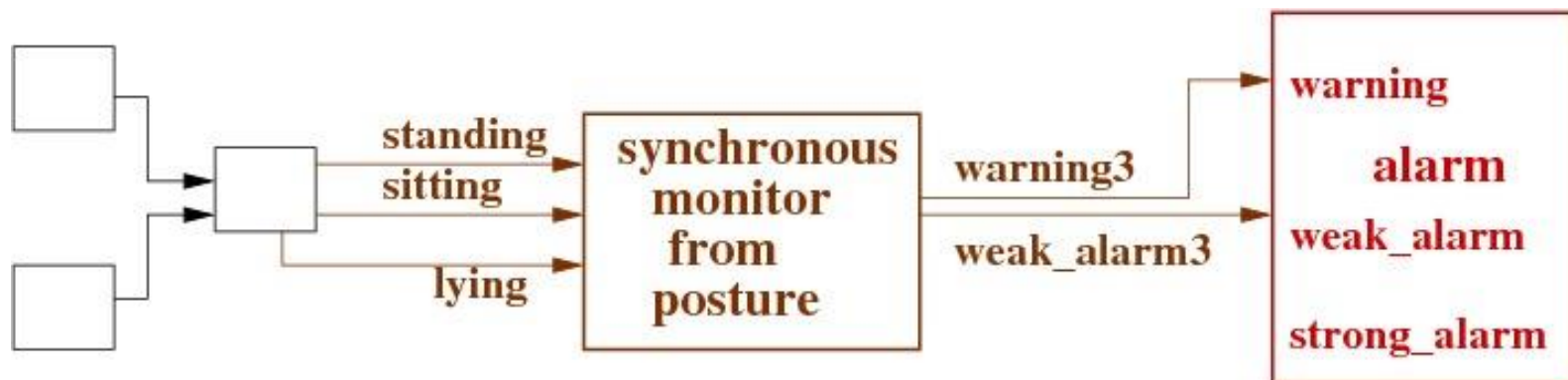


- **Use case:** observe kitchen usage
 1. **Camera** sensor (to locate the person)
 2. **Fridge** (contact sensor on the door) and a timer to know how long the door is opened
 3. **Posture** sensor (accelerometers) to know if the person is standing, sitting or lying
- **Goal:** send the appropriate alarm (strong, weak or warning)

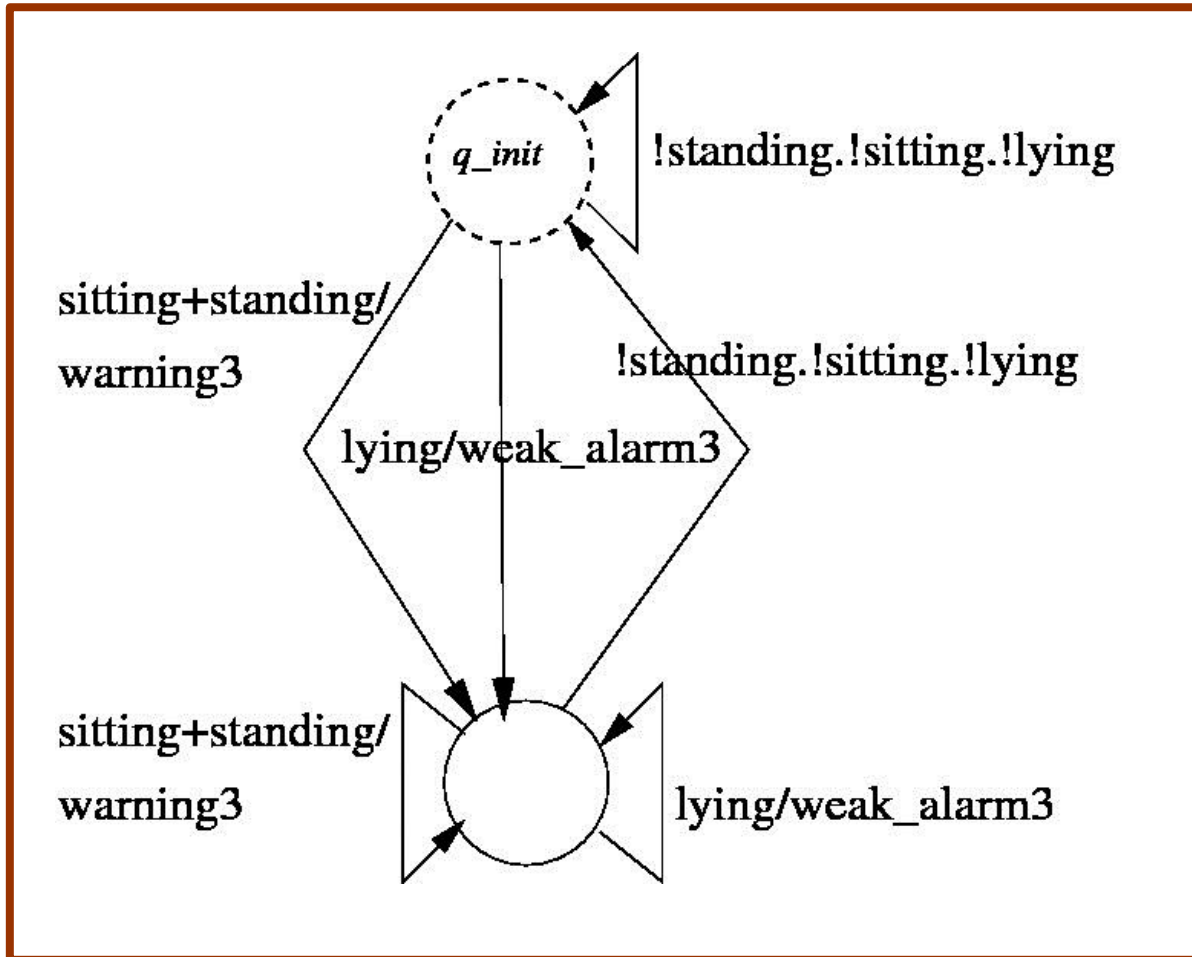
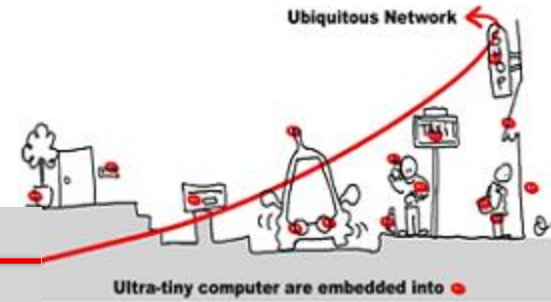
Use Case Implementation



- The **Alarm**, component is critical, 3 synchronous monitors will be introduced to specify the Alarm component behaviors w.r.t the fridge, the posture and the camera components

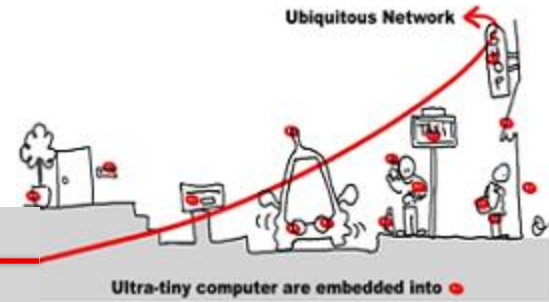


Use Case Implementation



Posture
synchronous
monitor

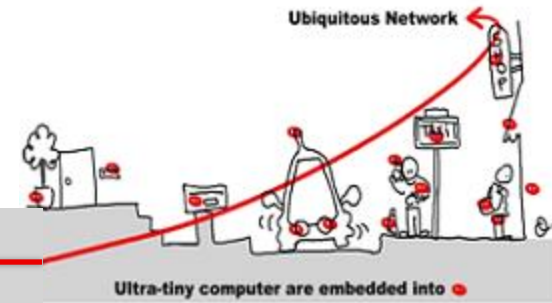
The SCADE solution



- How design the posture component ?
- How validate its behaviors ?
- How introduce it in the overall design ?

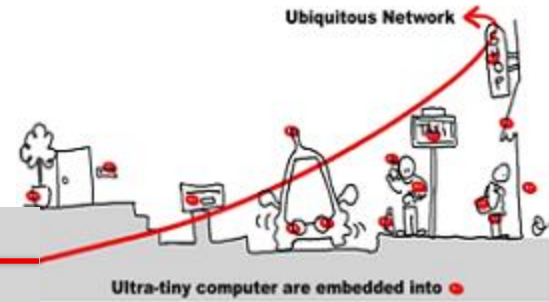
Rely on **SCADE** tool

SCADE: Safety-Critical Application Development Environment



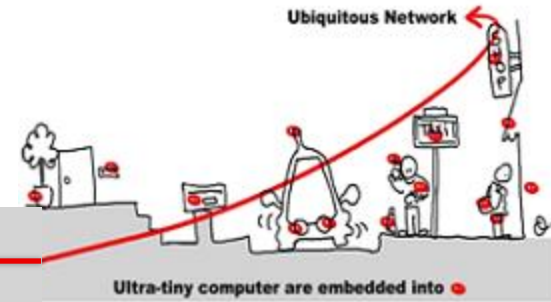
- Scade has been developed to address safety-critical embedded application design
- The Scade suite KCG code generator has been qualified as a development tool according to DO-178B norm at level A.

SCADE



- Scade has been used to develop, validate and generate code for:
 - avionics:
 - Airbus A 341: flight controls
 - Airbus A 380: Flight controls, cockpit display, fuel control, braking, etc,..
 - Eurocopter EC-225 : Automatic pilot
 - Dassault Aviation F7X: Flight Controls, landing gear, braking
 - Boeing 787: Landing gear, nose wheel steering, braking

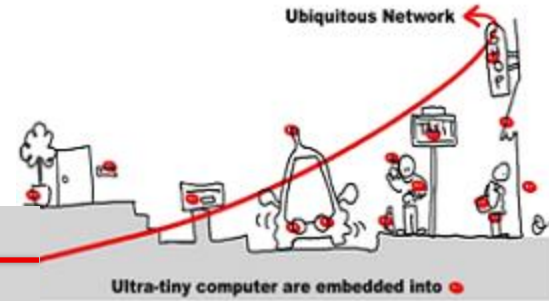
SCADE



- System Design
 - Both data flows and state machines
- Simulation
 - Graphical simulation, automatic GUI integration
- Verification
 - Apply observer technique
- Code Generation
 - certified C code



Modulo Counter



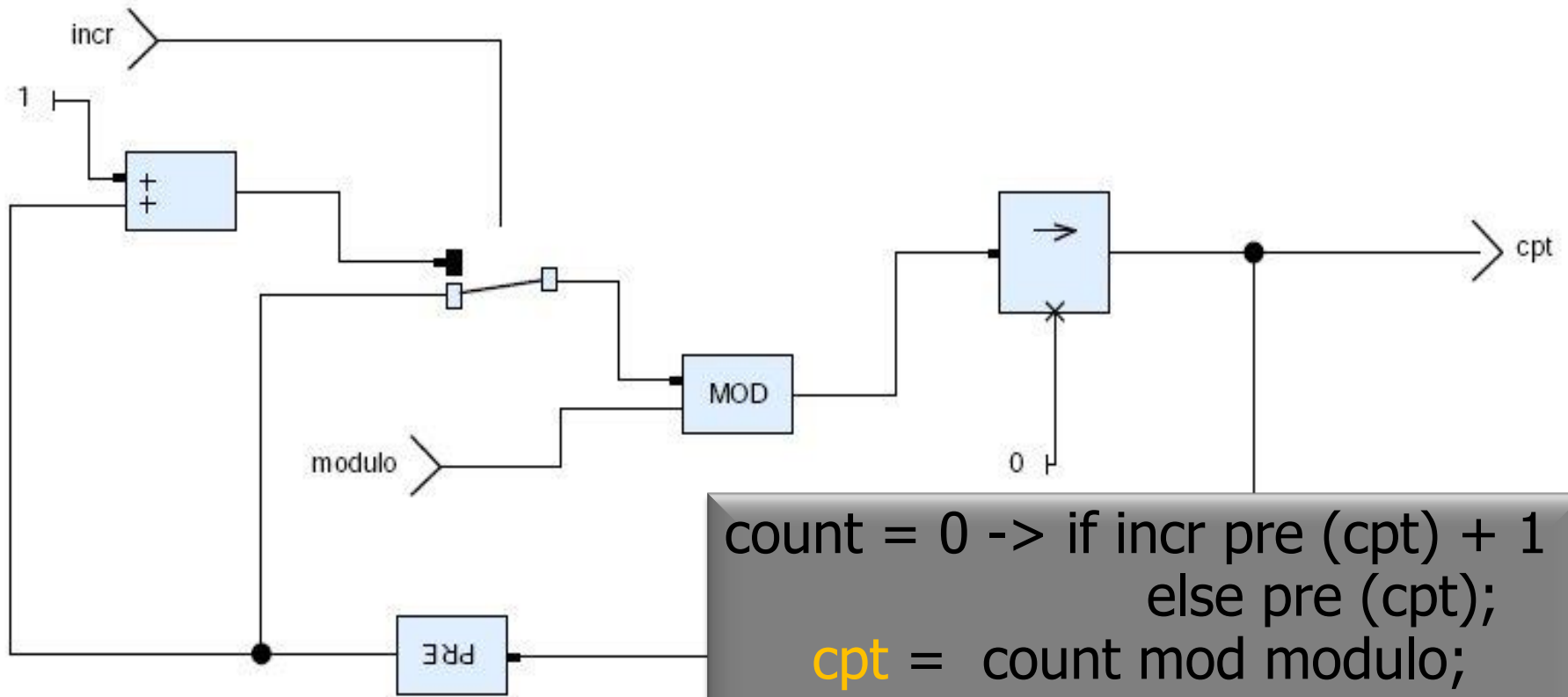
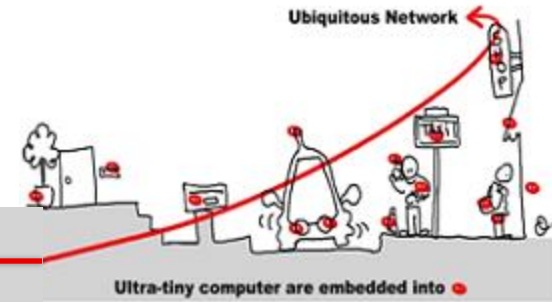
```
operator MCounter (incr:bool; modulo : int)  
    returns (cpt:int);
```

```
var count : int;
```

```
count = 0 -> if incr pre (cpt) + 1  
             else pre (cpt);
```

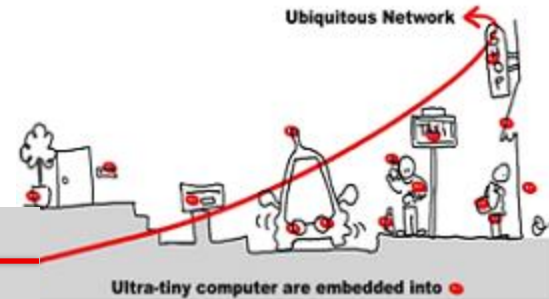
```
cpt = count mod modulo;
```

Modulo Counter



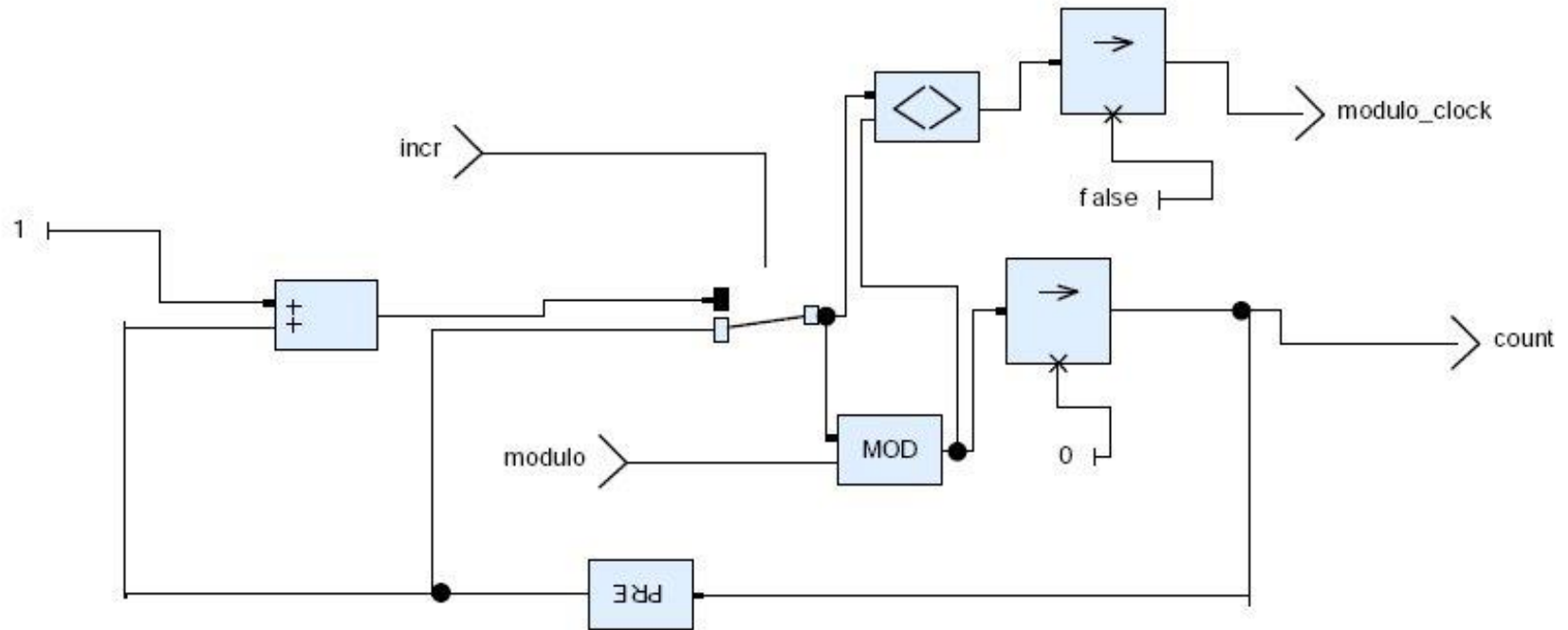
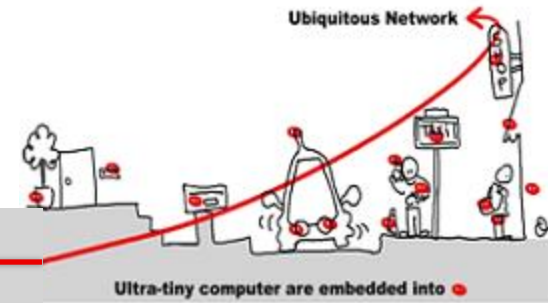
```
count = 0 -> if incr pre (cpt) + 1  
              else pre (cpt);  
cpt = count mod modulo;
```

Modulo Counter Clock

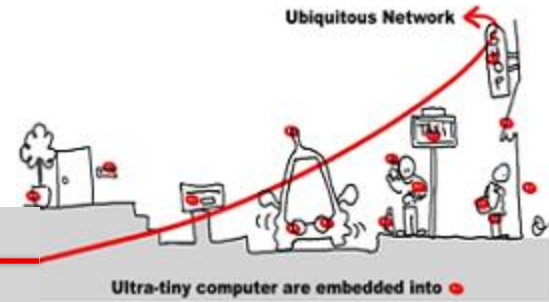


```
operator MCounterClock (incr:bool;  
                        modulo : int)  
    returns(cpt:int;  
           modulo_clock: bool);  
  
var count : int;  
count = 0 -> if incr pre (cpt) + 1  
             else pre (cpt);  
cpt = count mod modulo;  
modulo_clock = count <> cpt;
```

Modulo Counter Clock



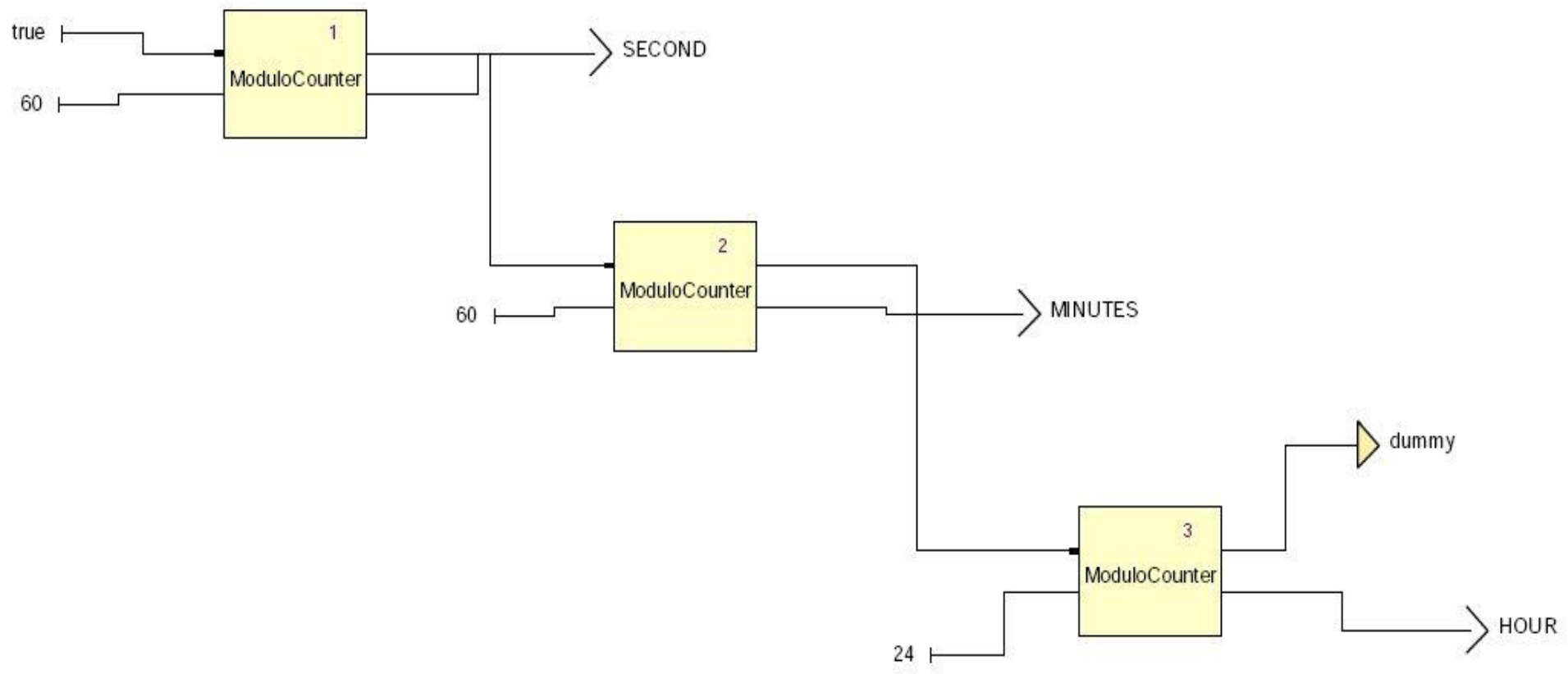
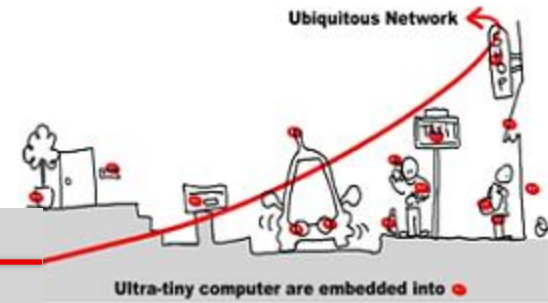
Timer



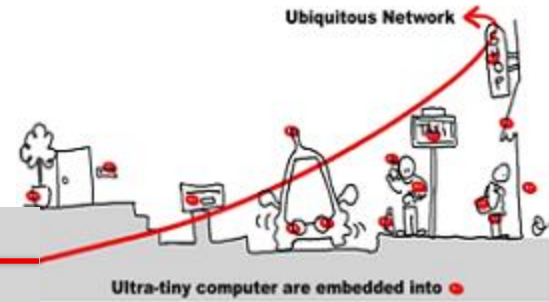
```
operator Timer returns (hour, minute, second:int);  
var hour_clock, minute_clock, day_clock : bool;
```

```
(second, minute_clock) = MCounterClock(true, 60);  
(minute, hour_clock) =  
    MCounterClock(minute_clock, 60);  
(hour, dummy_clock) =  
    MCounterClock(hour_clock, 24);
```

Timer

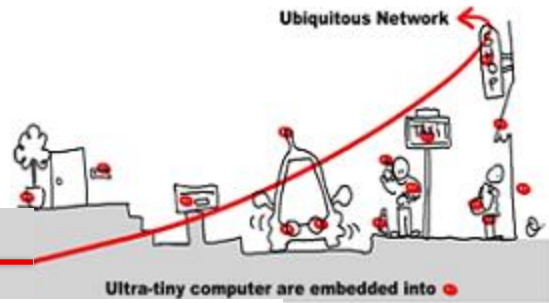


SCADE: state machines

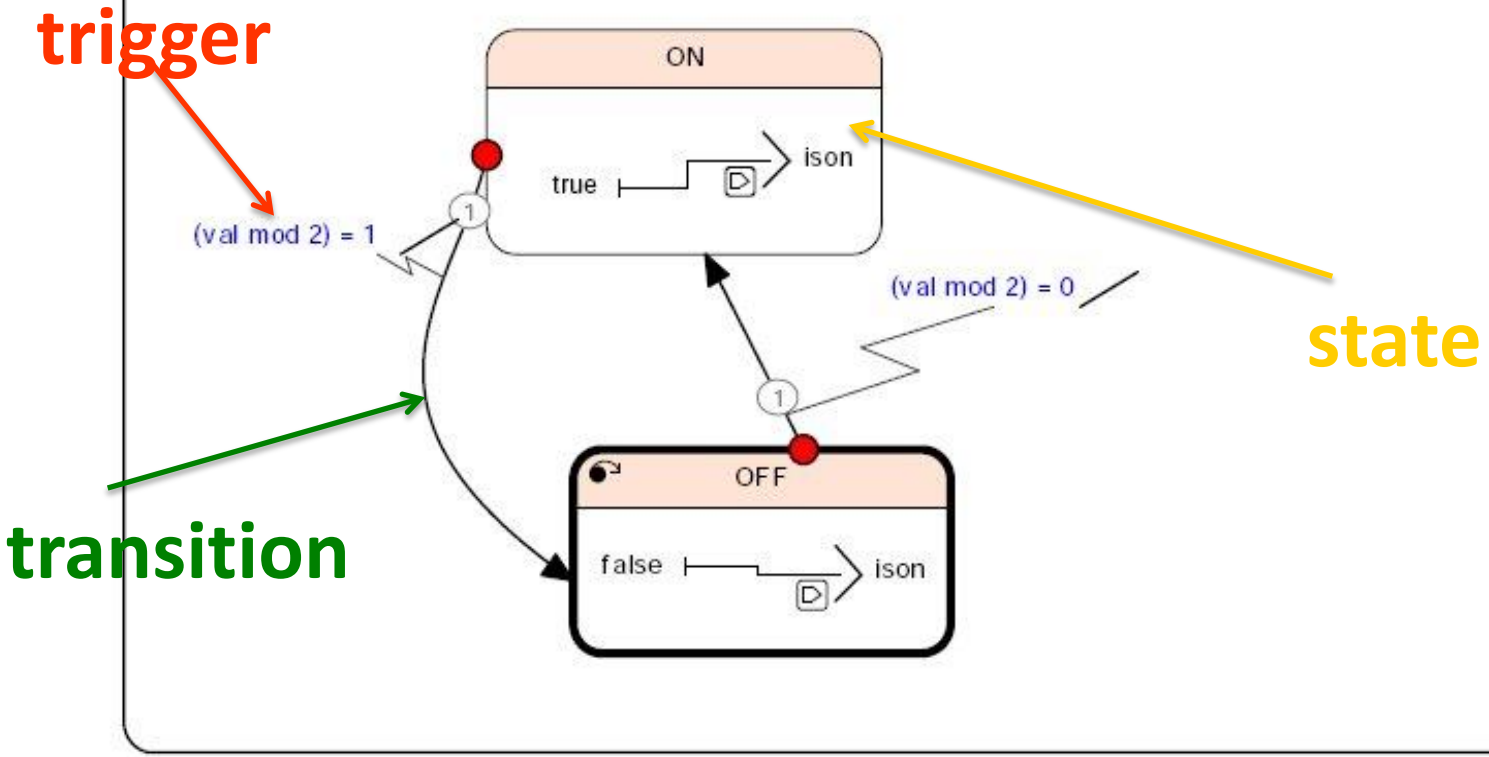


- Input and output: same interface
- States:
 - Possible hierarchy
 - Start in the initial state
 - Content = application behavior
- Transitions:
 - From a state to another one
 - Triggered by a Boolean condition

SCADE: state machines

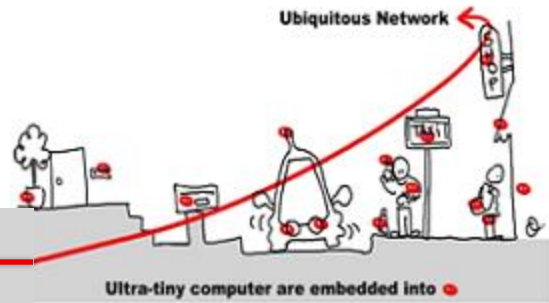


When ON, ison = true



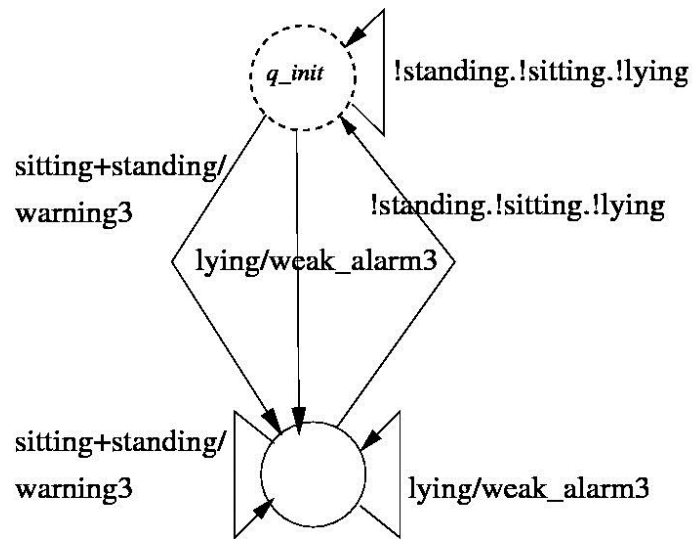
When off, ison = false

SCADE: model checking

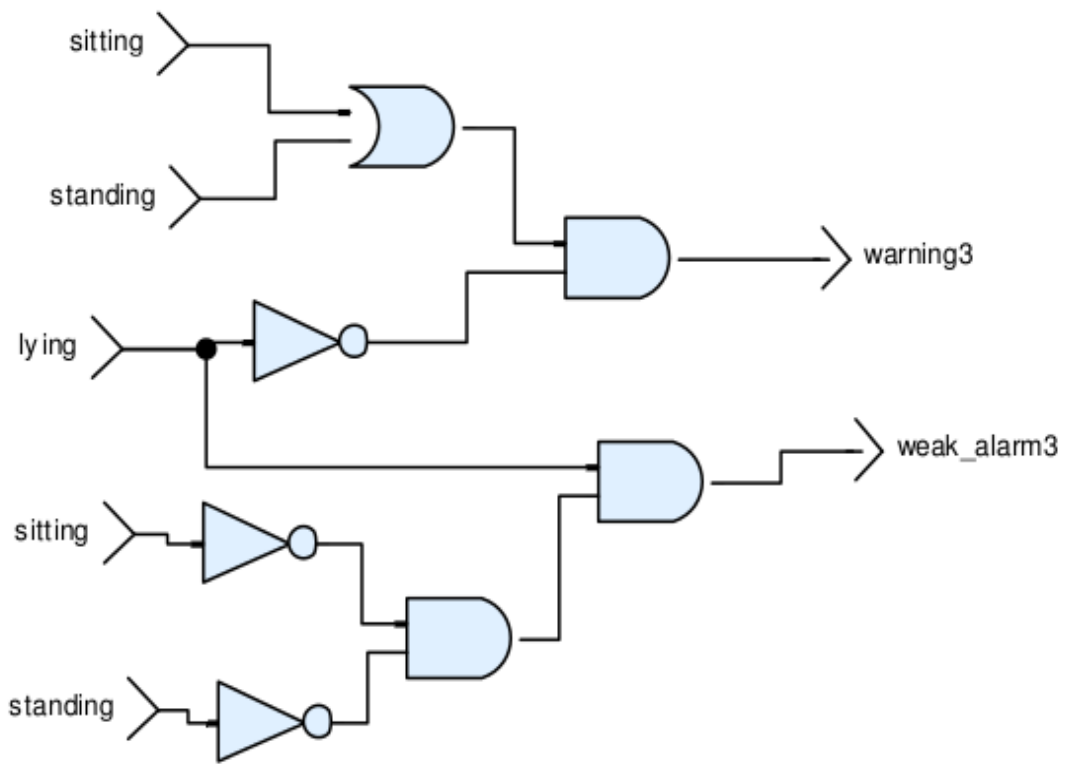


Observer technique

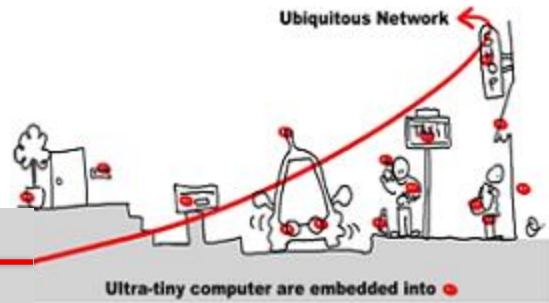
posture model



posture model specification in scade

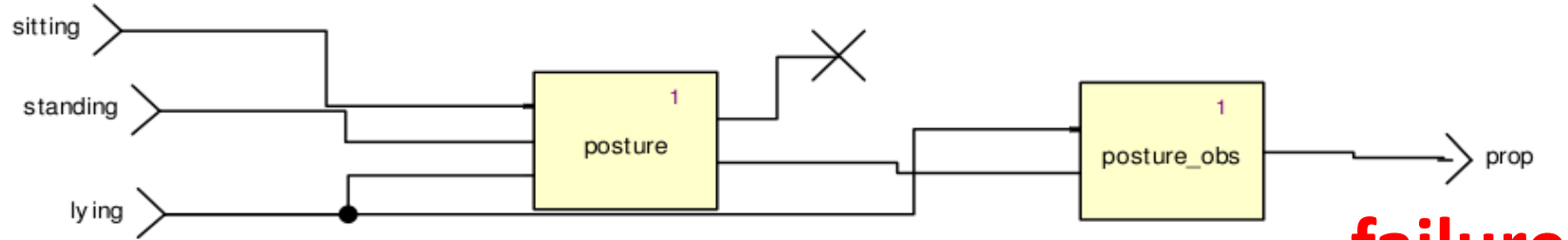
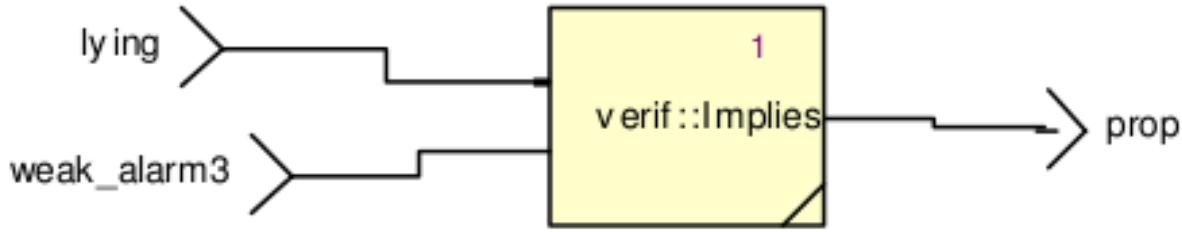


SCADE: model checking



Observer technique

posture
observer

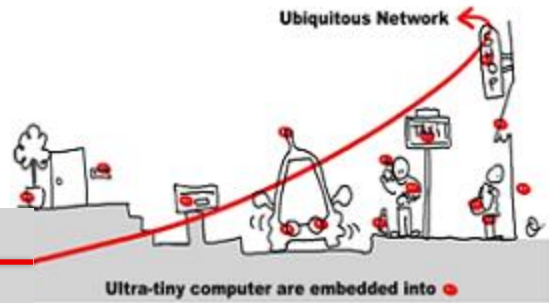


failure

posture verification

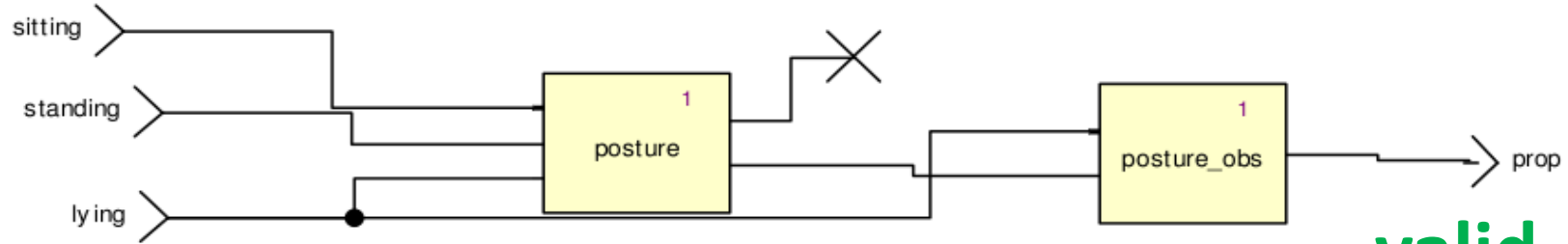
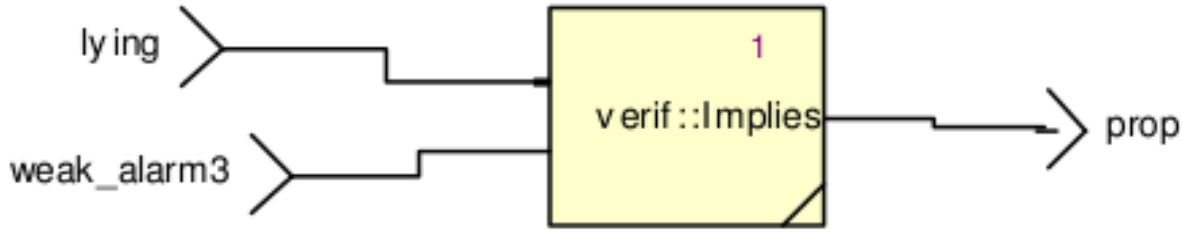
lying: true; sitting:true;standing:true

SCADE: model checking



Observer technique

posture
observer

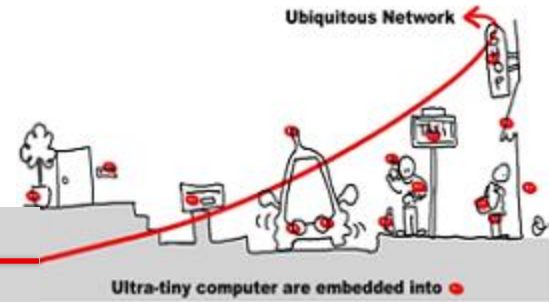


valid

posture verification

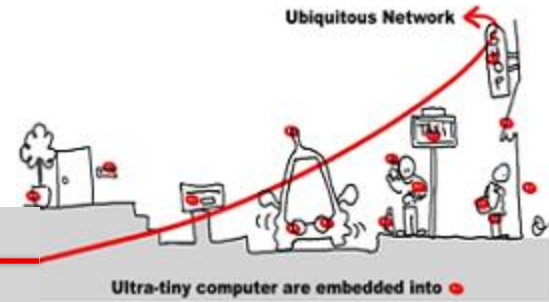
assume (lying # sitting # standing)

SCADE: code generation



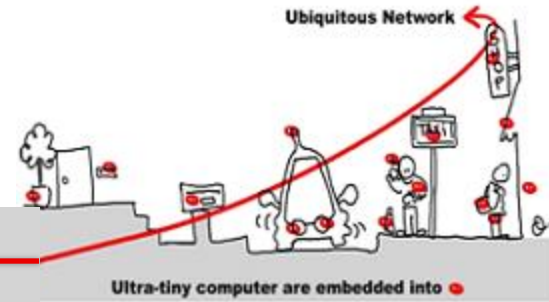
- KCG generates certifiable code (DO-178 compliance)
- Clean code, rigid structure (easy integration)
- Interfacing potential with user-defined code (c/c++)

SCADE: code generation structures



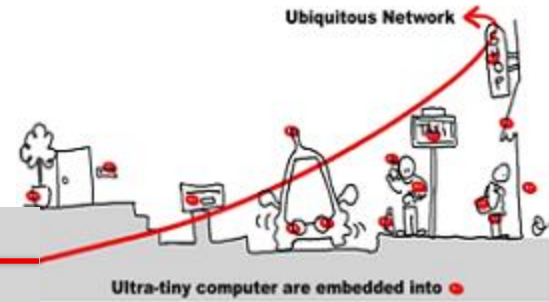
- `InC_<operator_name>`
 - structure C
 - one member for each input
- `OutC_<operator_name>`
 - Structure C
 - one member for each output and each state
 - Other members for output/state computations

SCADE: code generation structures



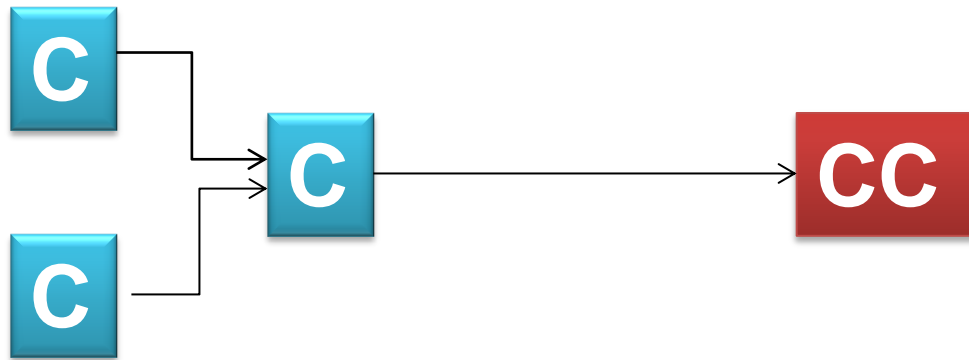
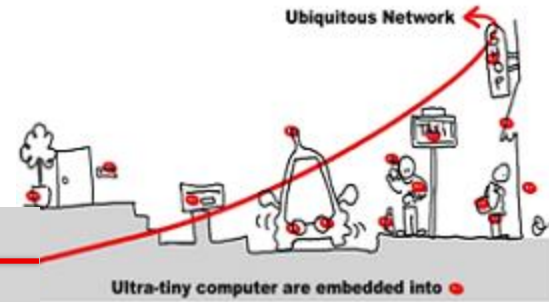
- Reaction function
 - for a transition (or a reaction) computes the output and the new state
 - `void <operator_name> (Inc_<operator_name> * inC, outC_<operator_name>* outc)`
- Reset function
 - To reset the reaction and the structures
 - `void <operator_name>_reset (outC_<operator_name>* outc`

SCADE: code generation files

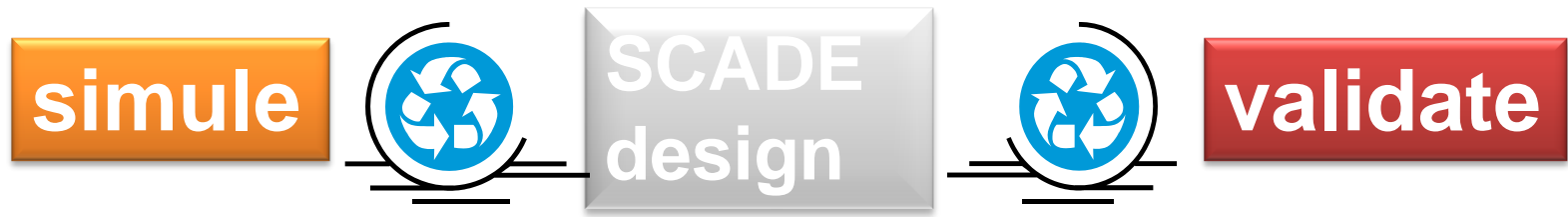
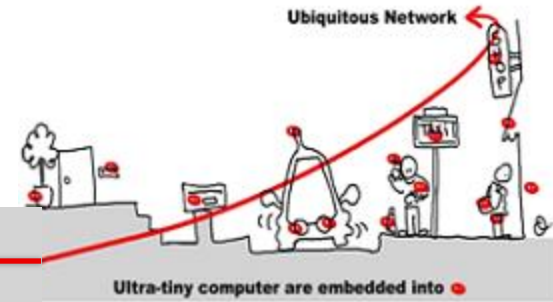


- Generated files
 - `<operator_name>.h` : type and function declarations for code integration
 - `<operator_name>.c` : implementation of reaction and reset functions
 - `kcg_types.(h,c)` to define types in C
 - `kcg_conts.(h,c)` to define constants

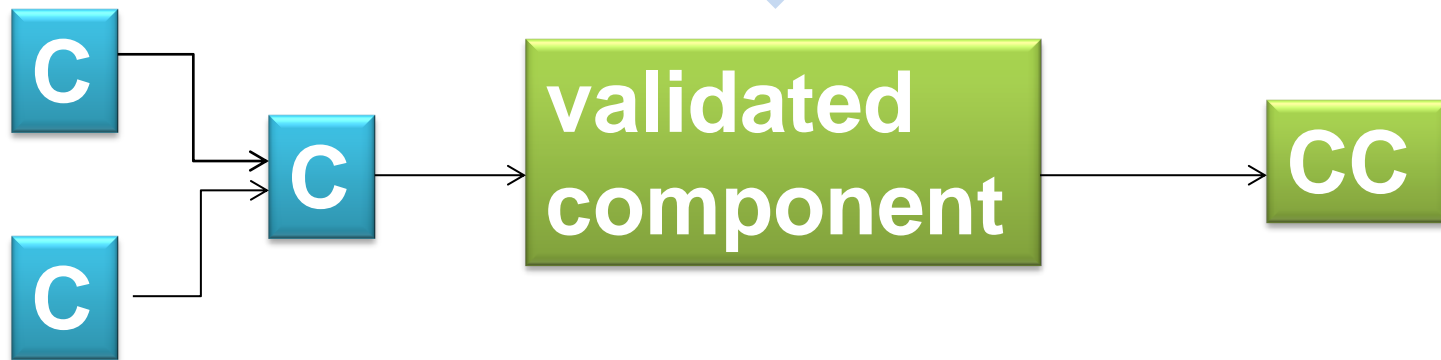
Critical Component Validation with SCADE



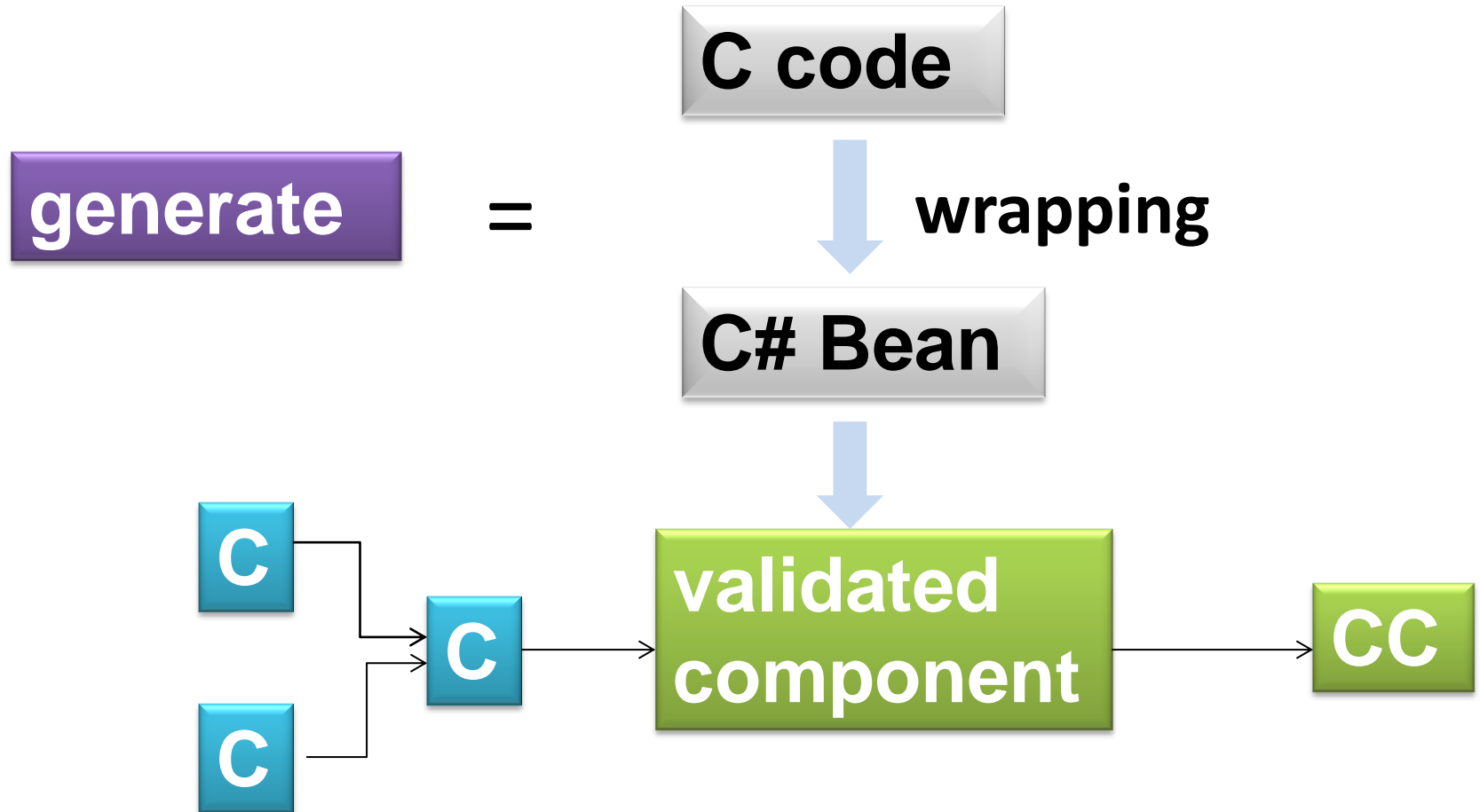
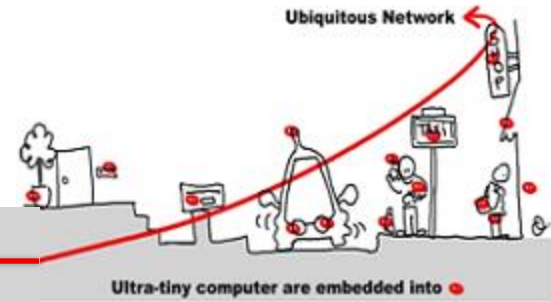
Critical Component Validation with SCADE



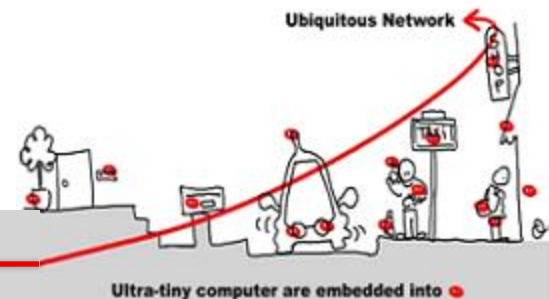
generate



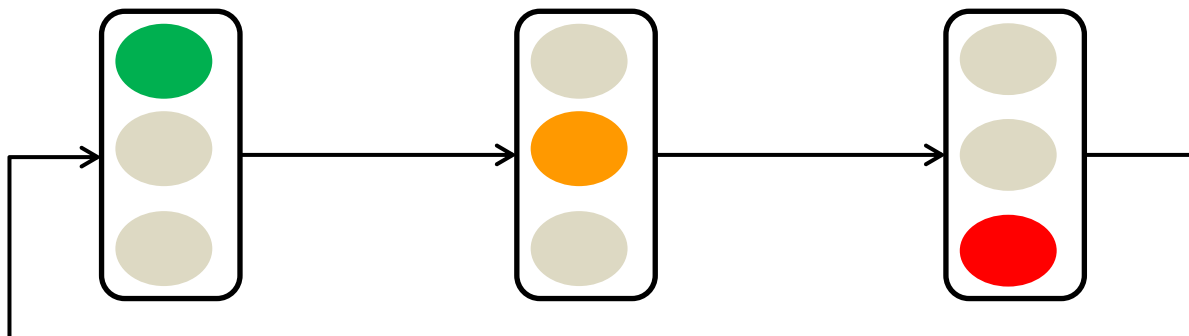
Critical Component Validation with SCADE for WComp



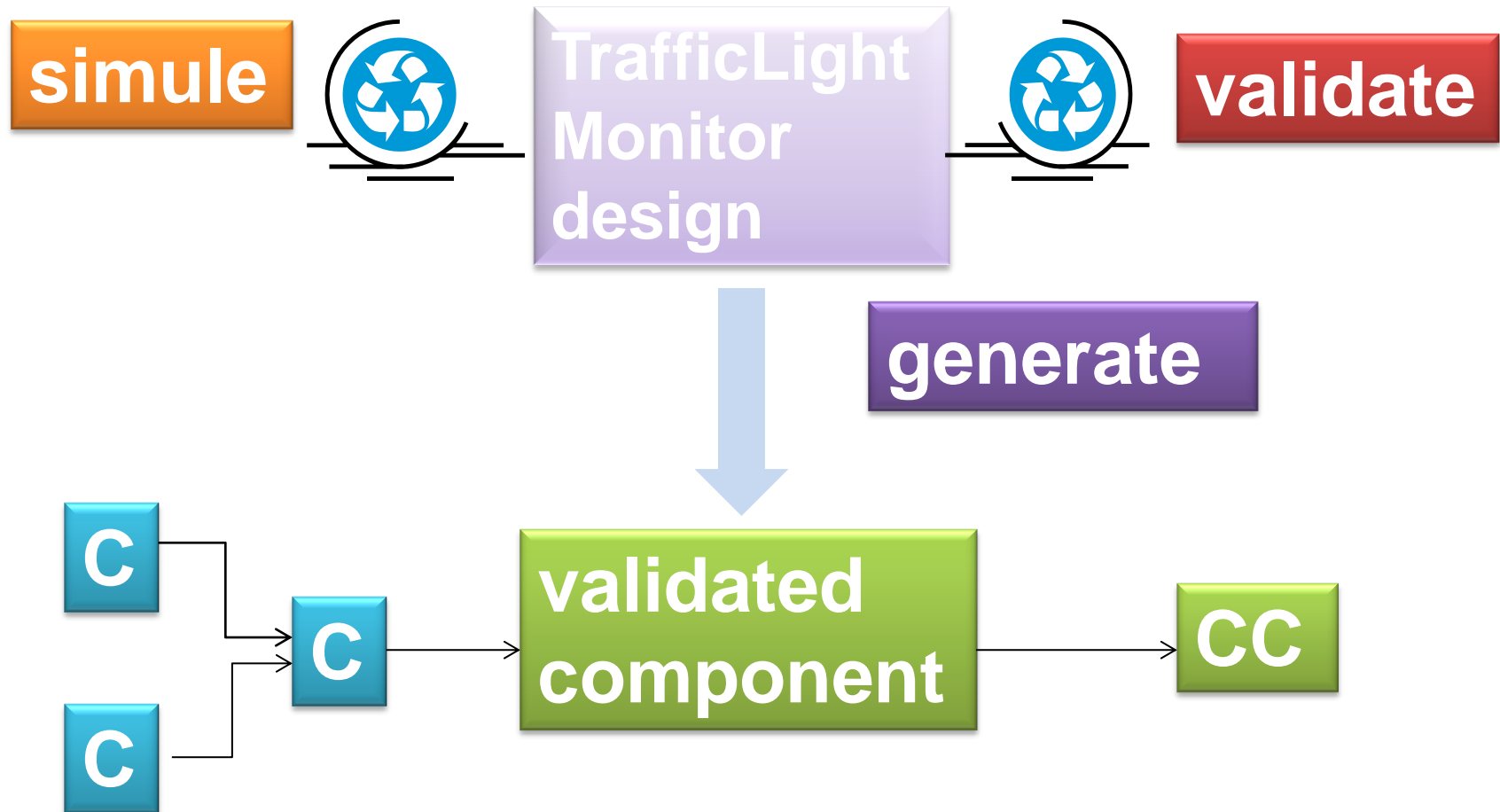
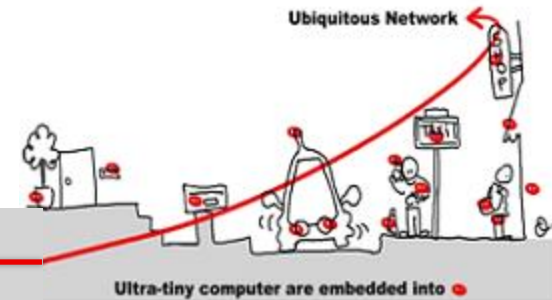
Example: TrafficLight Design in Wcomp Middleware



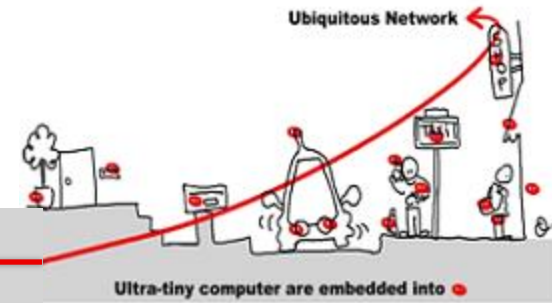
- Design a TrafficLight in WComp:
 1. Specify a TrafficLight synchronous monitor with Scade:
 - 3 lights : green, orange, red
 - Switch from green to orange, orange to red, red to green
 2. Connect the monitor to TrafficLight Wcomp component



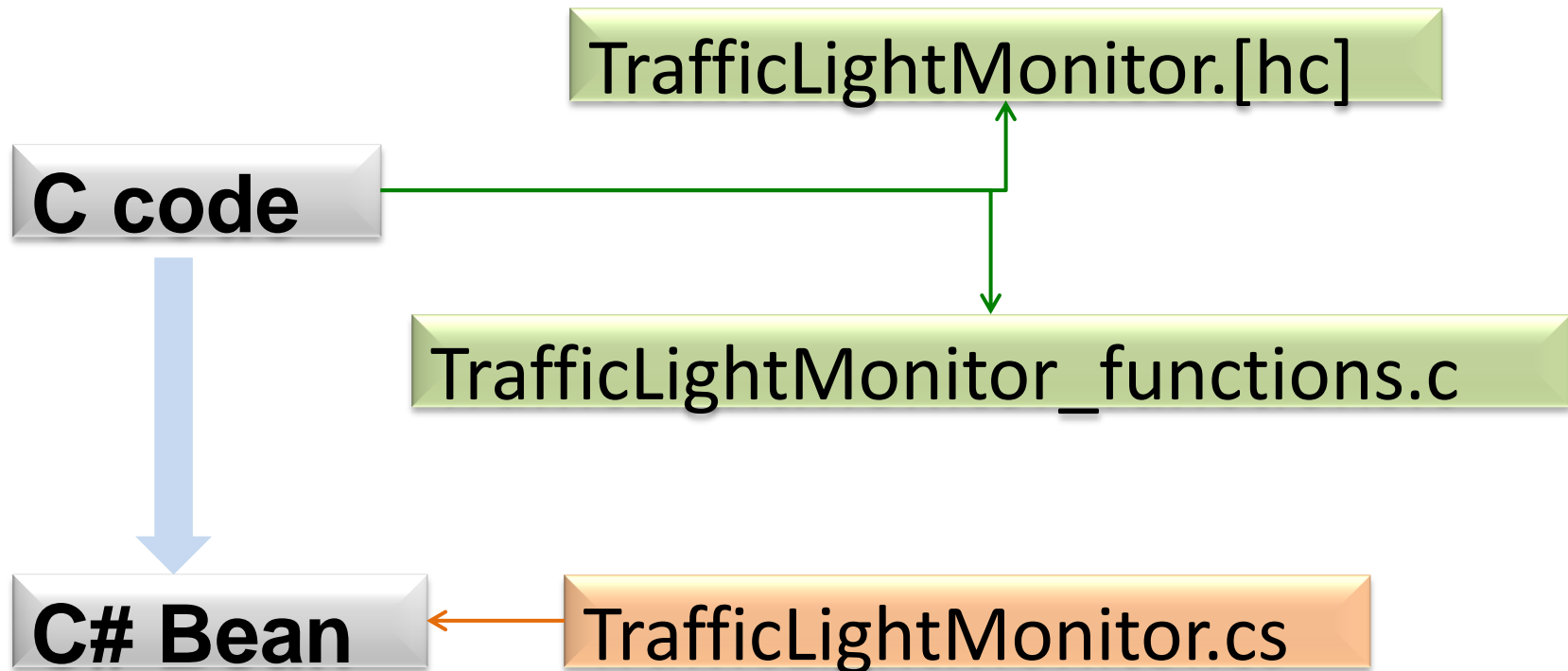
Example: TrafficLight Design in Wcomp Middleware



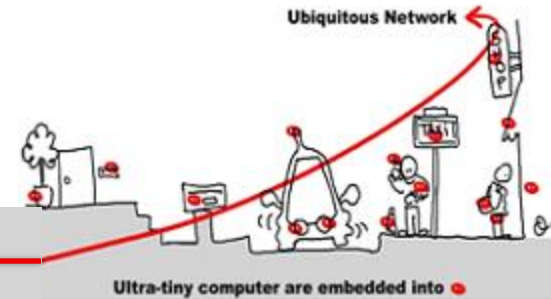
Example: TrafficLight Design in Wcomp Middleware



Generate TrafficLight Monitor Bean



Example: TrafficLight Design in Wcomp Middleware



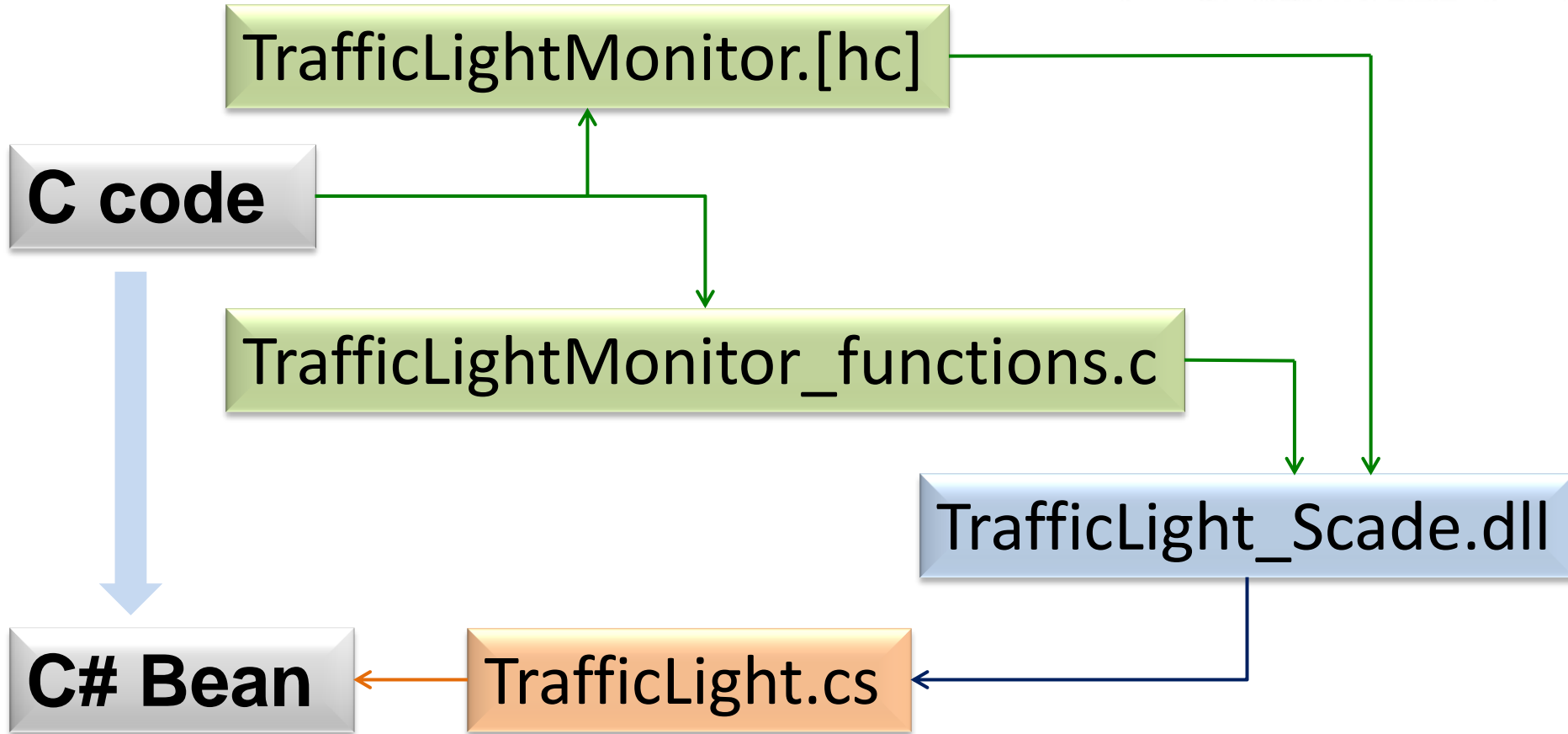
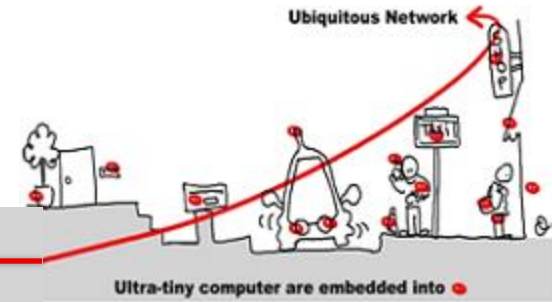
❖ TrafficLightMonitor.[hc]:

- ❖ Generated from scade design
- ❖ outC_TrafficLight structure containing an entry for each output of TrafficLight (*green, red, orange*)
- ❖ TrafficLight to perform a step in the automaton.

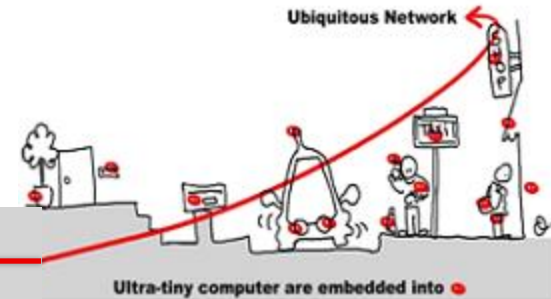
❖ TrafficLightMonitor_functions.c:

- ❖ User supplied
- ❖ Export structures and functions defined in TrafficLight.c
- ❖ Define a function to allocate outC_TrafficLight structure
- ❖ Define functions to get output respective values
ex: `get_green(outC_TrafficLight* out)`

Example: TrafficLight Design



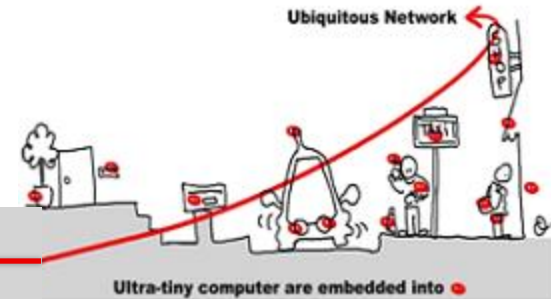
Example: TrafficLight Design in Wcomp Middleware



❖ TrafficLightMonitor.cs:

- ❖ Define class **TrafficLightMonitorBean** as extension of **EventedDrawable** Wcomp bean.
- ❖ Import functions from TrafficLight_Scade.dll
- ❖ Bean starting method: **TrafficLightMonitorBean** creates the output structure
- ❖ Step function: **doStep**:
 - ❖ Call of step function of the TrafficLightMonitor_Scade dll
 - ❖ Get the respective values of green, red and orange from the output structure

Example: TrafficLight Design in Wcomp Middleware



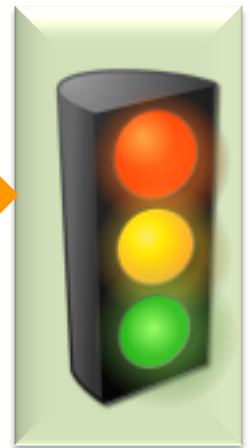
❖ TrafficLightMonitor.cs:

- ❖ Definition of events: RedChanged, RedOffChanged, GreenChanged, GreenOffChanged, OrangeChanged, OrangeOffChanged connected to methods of TrafficLight Wcomp bean:

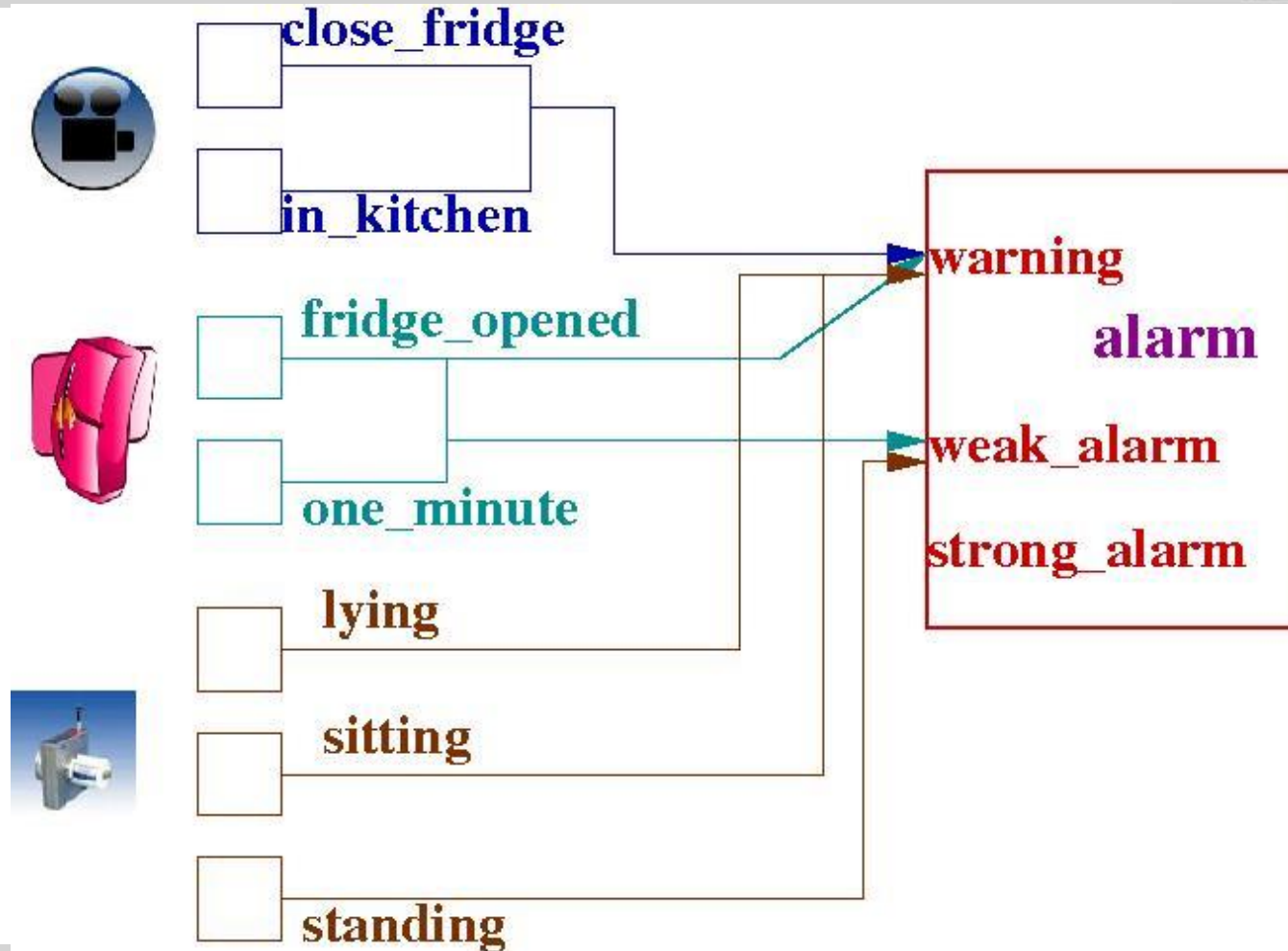
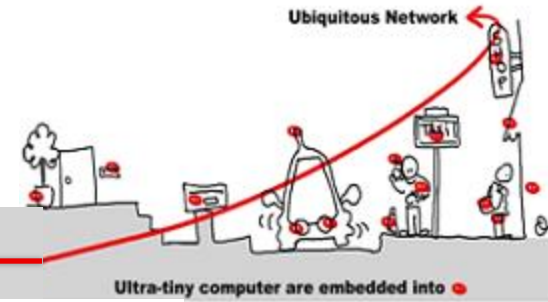


RedChanged → RedOn()
RedOffChanged → RedOff()
GreenChanged → GreenOn()

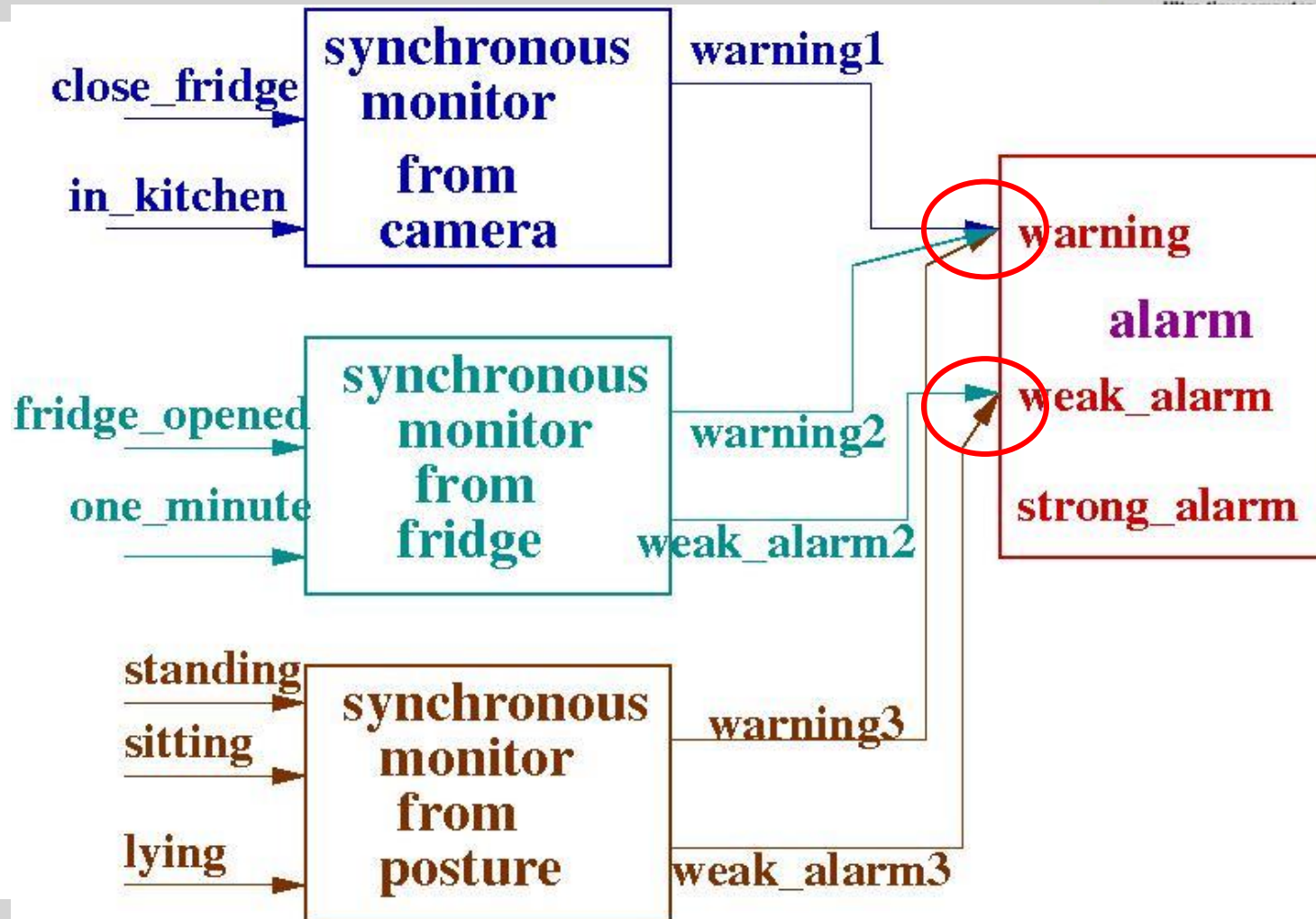
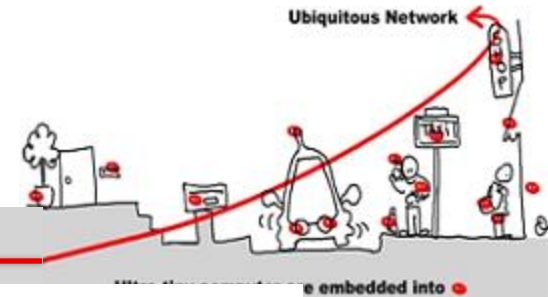
GreenOffChanged → GreenOff()
OrangeChanged → YellowOn()
OrangeOffChanged → YellowOff()



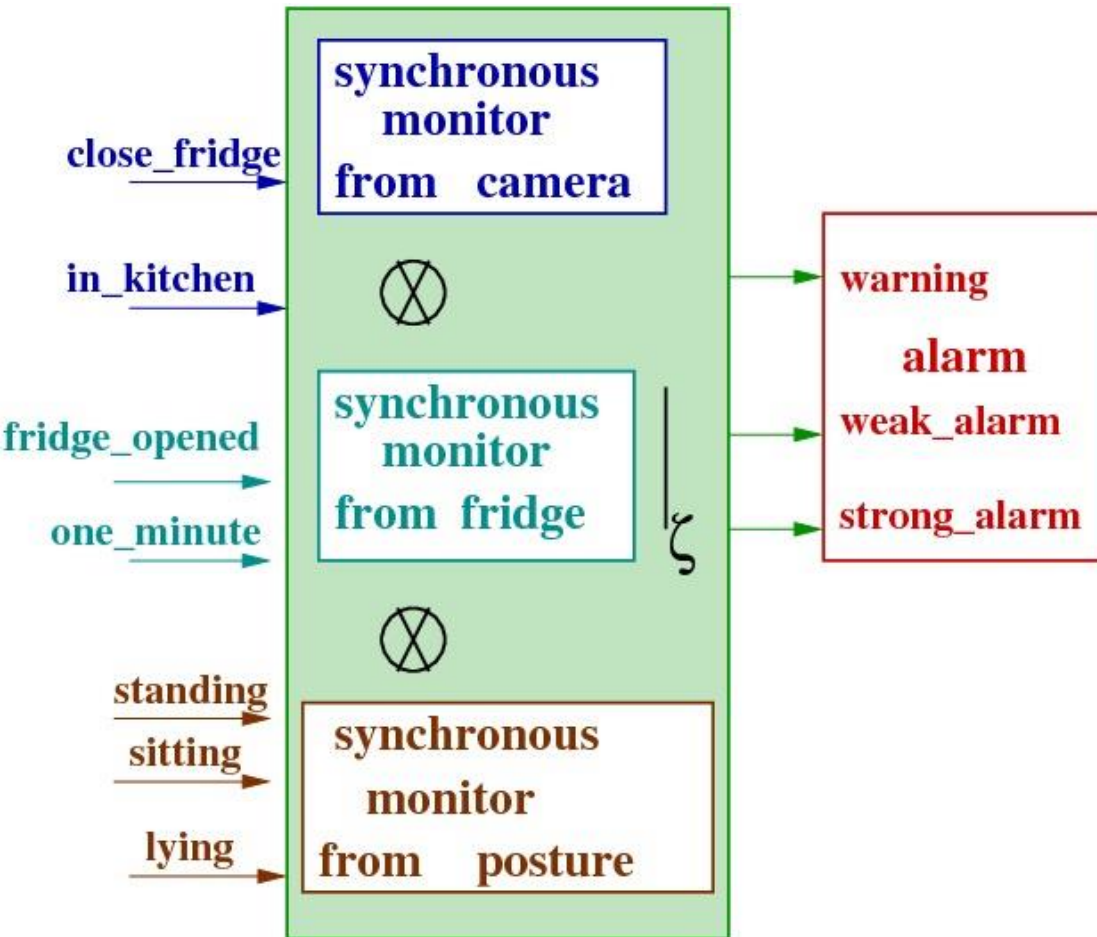
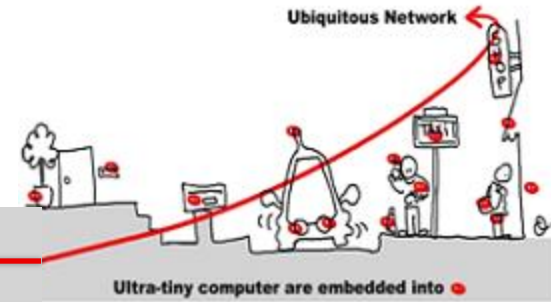
Synchronous Monitor Composition



Synchronous Monitor Composition

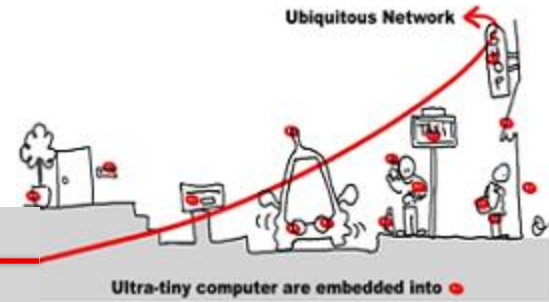


Synchronous Monitor Composition



Solution:
composition under constraint : $\otimes | \zeta$

Synchronous Monitor Composition



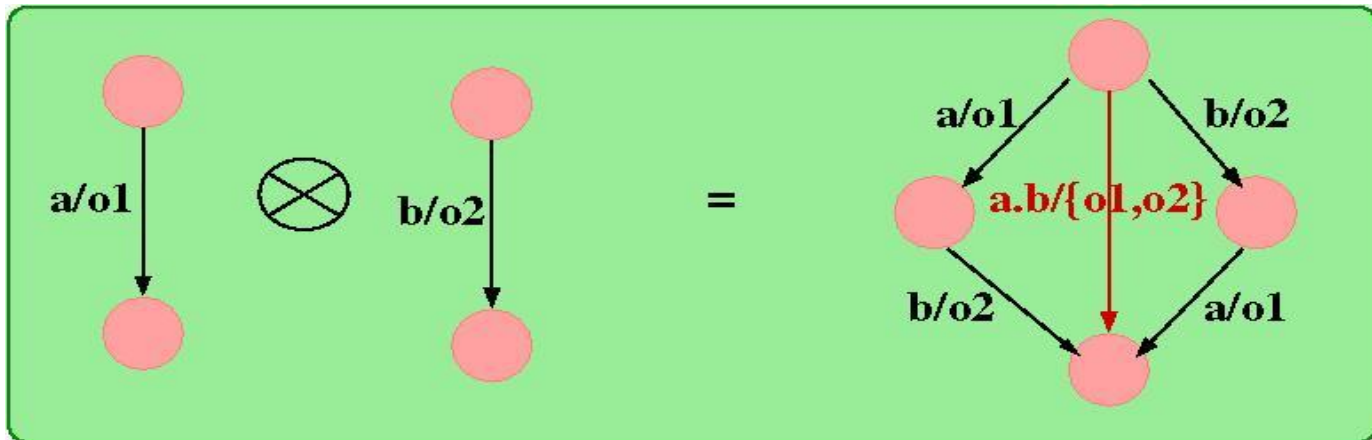
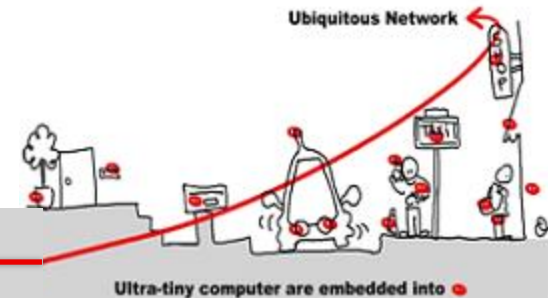
$\otimes|_{\zeta}$ = synchronous product +
constraint function

The constraint function tells us how multiple
accesses are combined

Property : $\otimes|_{\zeta}$ preserves safety property:

M_1 verifies Φ then $M_1 \otimes|_{\zeta} M_2$ verifies Φ also

Synchronous Monitor Composition

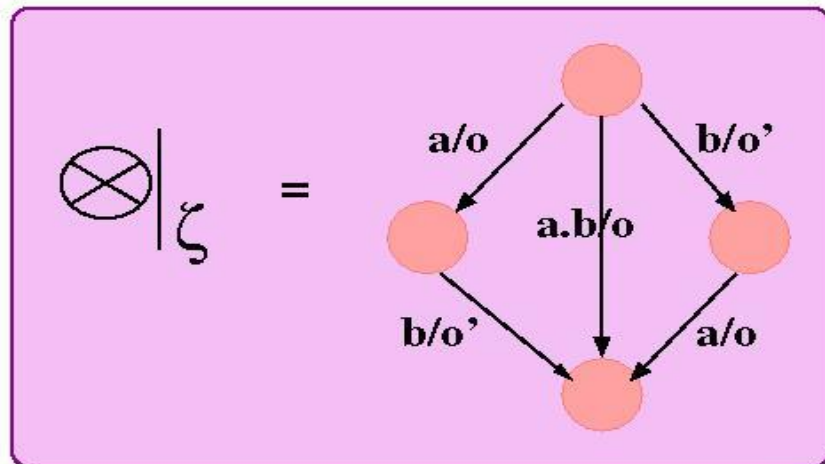


$$O = \{o, o'\}$$

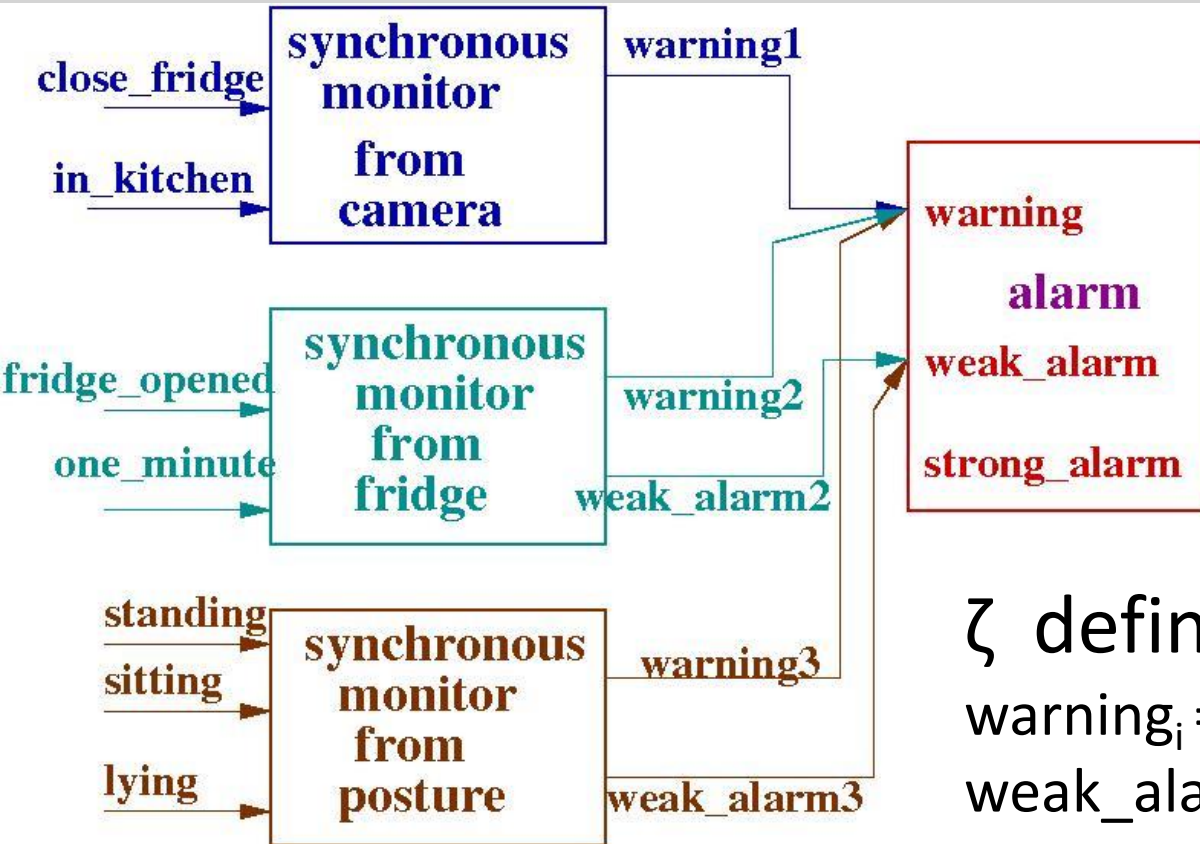
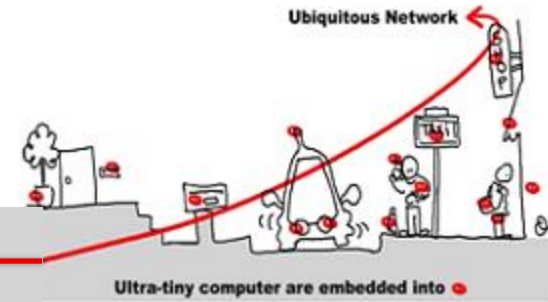
$$\zeta: o1 \rightarrow o$$

$$o2 \rightarrow o'$$

$$\{o1, o2\} \rightarrow o$$



Synchronous Monitor Composition

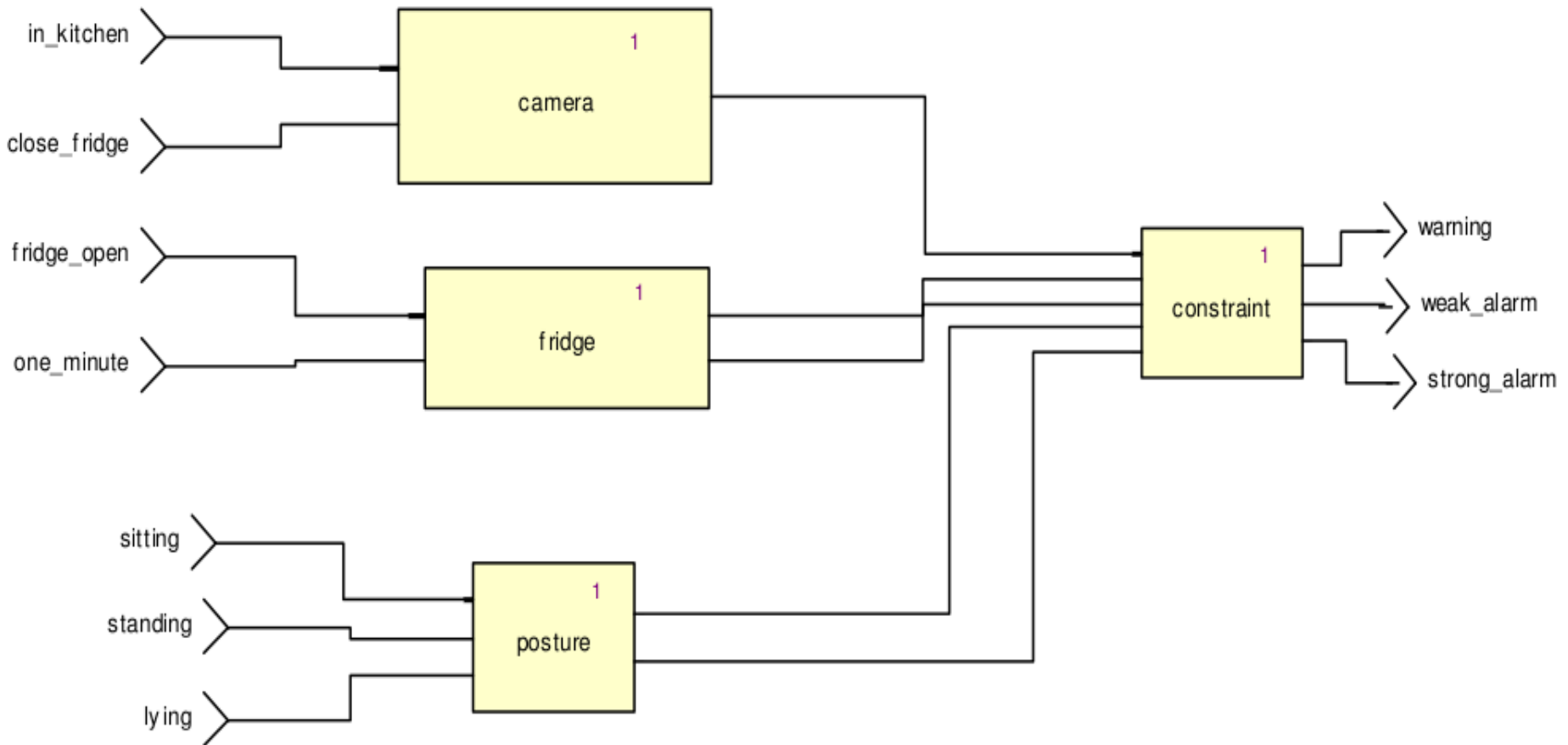
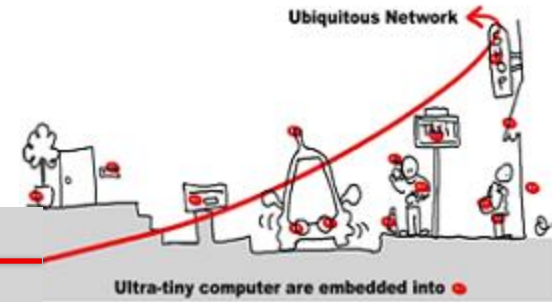


ζ definition:

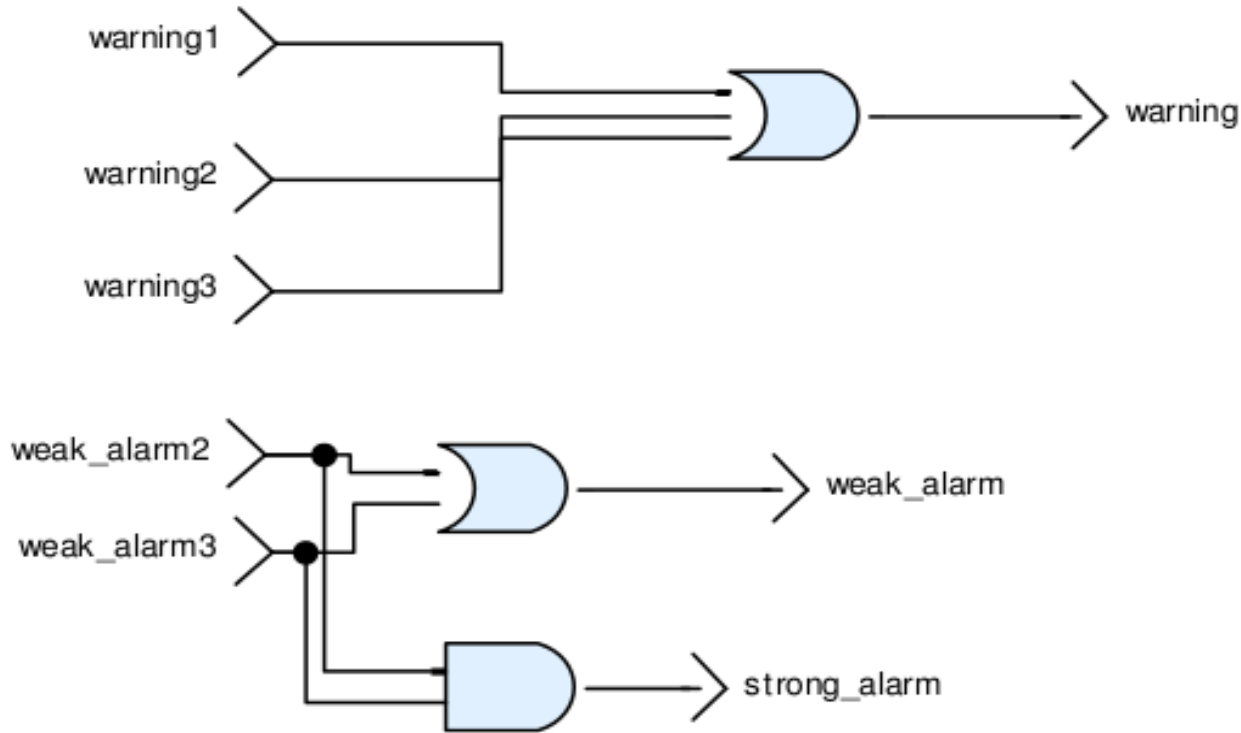
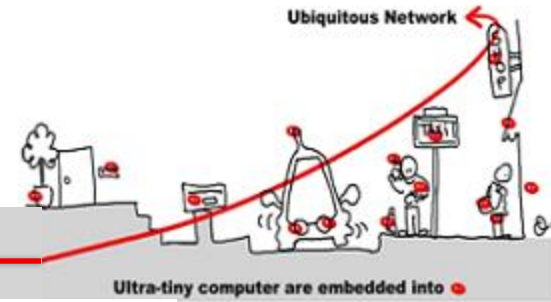
$warning_i = warning$

$weak_alarm_2 \ \& \ weak_alarm_3 = strong_alarm$

Synchronous Monitor Composition

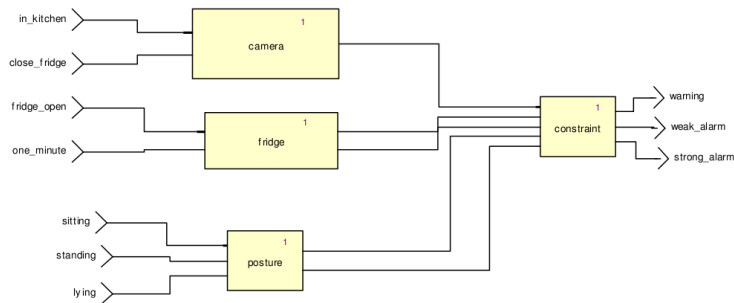
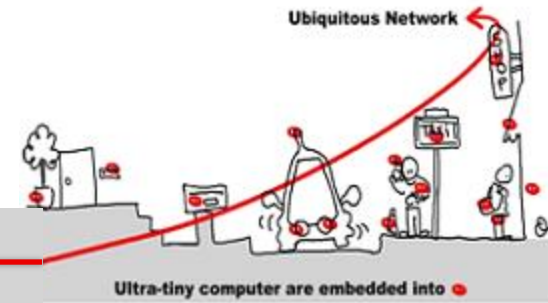


Synchronous Monitor Composition



$\text{weak_alarm}_2 \ \& \ \text{weak_alarm}_3$ implies strong_alarm

Use case Implementation in WComp



**validated
alarm Bean**

